

# Four-dimensional address topology for circuits with stacked multilayer crossbar arrays

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**We present a topological framework that provides a simple yet powerful electronic circuit architecture for constructing and using multilayer crossbar arrays, allowing a significantly increased integration density of memristive crosspoint devices beyond the scaling limits of lateral feature sizes. The truly remarkable feature of such circuits, which is an extension of the CMOL (Cmos + MOlecular-scale devices) concept for an area-like interface to a three-dimensional system, is that a large-feature-size complementary metal-oxide-semiconductor (CMOS) substrate can provide high-density interconnects to multiple crossbar layers through a single set of vertical vias. The physical locations of the memristive devices are mapped to a four-dimensional logical address space such that unique access from the CMOS substrate is provided to every device in a stacked array of crossbars. This hybrid architecture is compatible with digital memories, field-programmable gate arrays, and biologically inspired adaptive networks and with state-of-the-art integrated circuit foundries.**

digital memory | hybrid circuits | three-dimensional integrated circuits

**B**uilding three-dimensional circuits is a natural but so far limited way of increasing integration density to circumvent the inevitable stall in lateral device scaling (1, 2). One of the major challenges for any such system is to maintain a sufficiently high density of vertical interconnect to provide high-bandwidth and low-latency communication to and from each layer in the stack without sacrificing so much area within each layer for vias to negate the advantages of stacking. In this article, we show how this problem can be avoided by using a hybrid complementary metal-oxide-semiconductor (CMOS)/crossbar circuit to implement an “area interface” that utilizes a four-element logical address to specify each physical memory device. Previous approaches to three-dimensional circuitry have been limited by the requirement to integrate active components up the vertical stack (3, 4). However, multilayer CMOS circuits have many obstacles—thin-film transistor technologies have poor performance characteristics for memory and logic applications, whereas three-dimensional wafer bonding suffers from low interconnect density because of limitations to alignment between wafers (i.e., as compared with that of photolithographic masks defining features on a single wafer for multiple metallization layers) and from poor cost efficiency (5).

Here, we describe an architecture, based on hybrid circuits composed of a conventional CMOS layer connected to multiple crossbar layers that contain memristive devices. A memristor is a two-terminal electrical circuit element that changes its resistance depending on the total amount of charge that flows through the device (6, 7). A memristance arises naturally in thin-film semiconductors for which electronic and dopant equations of motion are coupled in the presence of an applied electric field (8). This property is actually common for nanoscale films and has been observed in a variety of material systems (e.g., transition metal oxides and perovskites, various superionic conductors composed of chalcogenides and metal electrodes, and organic polymer films) (9, 10). Although memristance was observed experimentally for at least 50 years before it was recognized as such, it now has become interesting for a variety of digital and analog applications, especially

because a true memristor does not lose its state when the electrical power is turned off.

Other key advantages of memristive devices are their small footprints—on the order of  $4F^2$ , where  $F$  is the lithographic feature size (or half-pitch)—and relatively simple structures that are easily fabricated and integrated with conventional CMOS processes. However, memristive devices are not active components (e.g., the equivalent of the CMOS transistor), because they cannot supply energy to a circuit. The solution to that problem is to complement crossbar arrays of memristive devices with a conventional CMOS layer that provides signal restoration and gain but is much less dense. Such a concept, named CMOL (Cmos + MOlecular-scale devices), was proposed originally in the context of nonphotolithographic techniques (11) for a single crossbar layer (i.e., to make higher-density two-dimensional circuits). We show here how to construct hybrid circuits with multiple layers of crossbars that are all addressed with a single set of vertical vias to amplify the density advantage of the memristive switches. Each memory bit requires four labels to specify its location (the four-dimensional address) instead of the usual two required for two-dimensional arrays. The additional complexity in dealing with the larger logical address is more than compensated by the fact that the number of memristive devices that can be addressed scales as the fourth power of the number of transistors in the CMOS circuitry instead of the second power, which dramatically increases the number of devices that can be addressed within a fixed area. Various applications, such as digital memories, field-programmable gate arrays (FPGAs), and even some exotic applications, including synaptic networks, should benefit from this hybrid architecture.

**From Two-Dimensional to Three-Dimensional Hybrid Circuits.** Geometrically regular circuits, such as digital memories, even can be optimized efficiently without the use of design automation tools. For instance, Fig. 1A shows a typical array topology used for various memories that renders a simple and compact circuit layout. The memory device, represented by a green dot, depends on the type of technology (i.e., is it a capacitor, variable capacitor, floating gate transistor, four transistor feedback loop circuit, or magnetic tunnel junction in dynamic random access memory (RAM), ferroelectric RAM, flash, static RAM, or magnetoresistive RAM memories, respectively). The read/write operations may be unique for each memory technology, but in general a read operation involves sensing a physical quantity, such as charge, used to store state in a particular device. Accessing a particular memory device in a square array requires the selection of one word line and one bit line (out of  $N$  total each) to establish electrical connections between the desired memory cell and the peripheral input/output circuitry.

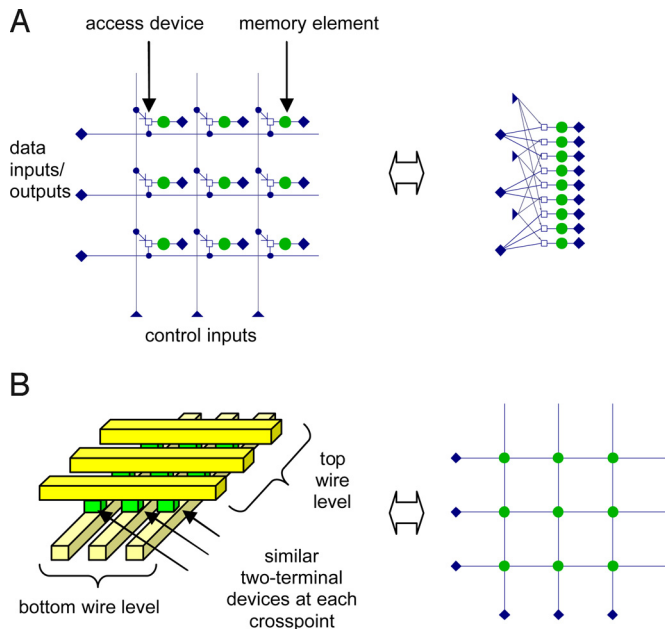
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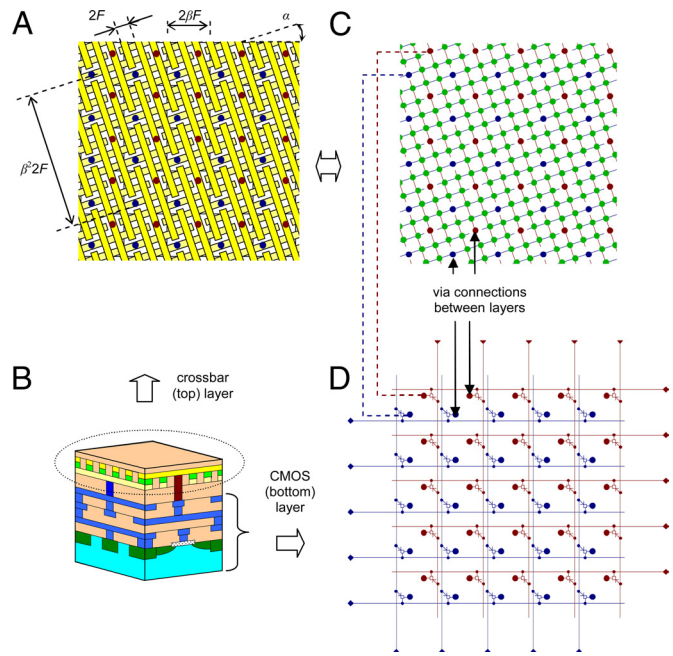
**Fig. 1.** Typical structures for (A) arrays with each cell having a dedicated access element (transistor) and (B) crossbar arrays with equivalent circuit representations used in the following discussion. The specific case  $n = 3$  is used for illustration, but practical arrays are much larger (e.g., to reduce peripheral overhead in memory applications).

Thus, the demultiplexing and multiplexing functions are performed with an “edge interface” that utilizes  $N$  channels on each of two sides of the array (for a total of  $2N$  channels) to access  $N^2$  memory cells using a two-label address. By integrating the access function into the crosspoint memory device, one can implement crossbar memory circuits (Fig. 1B). In the case considered here, the crosspoint device is a memristive element with a highly nonlinear current–voltage characteristic such that current flow can be detected by applying a full voltage bias across a specified junction while biasing the rest of the lines at half of that voltage to suppress the leakage currents (12).

Crossbar circuits have attracted a great deal of attention, because the device integration density is  $(2F)^{-2}$ , where  $F$  potentially can be scaled down to a few nanometers (12–17), whereas other types of memory devices that incorporate a transistor into each memory element require a larger area per device. In addition, even if  $F$  is set by optical photolithography (a few tens of nanometers), the bit density with  $M$  crossbar layers is  $M(2F)^{-2}$  (18). The greatest challenge is how to approach the maximum density that can be fabricated given the limited functionality of memristive devices and the overhead required for a CMOS addressing circuit and vias to connect the layers. An interesting solution to this problem, called CMOL (11, 19), was developed in the context of nanoscale crossbar circuits (Fig. 2). The key features in this hybrid solution are (i) an “area interface” between the CMOS and nanosystems, (ii) the crossbar array rotated by an angle  $\alpha$  with respect to the mesh of CMOS-controlled vias (20), and (iii) a double decoding scheme that provides unique access to each crosspoint device (11, 19).

More specifically, as Fig. 2 shows, two types of vias,\* one connecting to the lower (shown with blue dots) and the other to the upper (red dots) wire level in the crossbar, are arranged into a square array with side  $2\beta F$  (which is also equal to the side

\*Here, we specify typical metal via plugs (i.e., those used for connecting wires in adjacent metallization layers of the interconnect stack in conventional CMOS technology).



**Fig. 2.** Two-dimensional circuits with an area distributed interface. (A) Top view of the crossbar structure showing  $\alpha$  for  $r = 3$ . (B) Cut-away illustration showing the two types of vias connecting the CMOS control circuitry to the lower (blue) and upper (red) wire levels of the crossbar. (C, D) Corresponding equivalent circuit diagram for the  $n = 5$  primitive cell array using the notations from Fig. 1.

length of the “cells” grouping two vias of each kind). Here,  $\beta$  is a dimensionless number  $>1$  that depends on the cell size (i.e., complexity) in the CMOS subsystem. The crossbar is rotated by an angle  $\alpha = \arcsin(1/\beta)$  relative to the via array such that vias naturally subdivide the wires into fragments of length  $\beta^2 2F$ . The factor  $\beta$  is not arbitrary but is chosen from the spectrum of possible values  $\beta = (r^2 + 1)^{1/2}$ , where  $r$  is an integer so that the precise number of devices on the wire fragment is  $r^2 - 1 \approx \beta^2$ .

The decoding scheme in CMOL is based on two separate address arrays (one for each level of wire in the crossbar) with access devices similar to those shown in Fig. 1A meshed together. Fig. 2D shows that there are a total of  $4N$  edge channels (illustrated schematically with one edge channel on each of the four sides of the array) to provide access to two different via controllers (one blue and one red) in each of  $N^2$  addressing cells in the CMOS plane. In contrast to standard memory arrays, in CMOL each control and data line pair electrically connects the peripheral input/outputs to a via instead of a single memory element. In turn, each via is connected to a wire fragment in the crossbar. The two perpendicular sets of wire fragments provide unique access to any crosspoint device in a fashion similar to Fig. 1B, even for large values of  $\beta$ . The total number of crosspoint devices that can be accessed by the  $N \times N$  array of CMOS addressing cells is  $\approx N^2 \beta^2$ , which can provide a significant multiplicative factor when comparing CMOS to crossbar implementations, especially if the lithographic feature size of the crossbar is smaller than that of the CMOS. An alternate way of viewing this is that one can use complex CMOS circuitry built with a significantly larger feature size to address regular crossbars built at a much finer lithographic scale.

From the discussion so far, that the CMOS area interface of the CMOL architecture actually can address a much larger number of crosspoint devices than are present in the single crossbar may be obvious. The major contribution of this article is to show how large the address space actually is and how to use



the wire fragment size is independent of  $N$  and only defined by the parameter  $\beta$ . For example, assume that all of the crossbar wires are made with optical lithography and the cell consists of two access transistors serving the two vias. In this case,  $\beta \approx 5$  (12) and  $N \geq 10,000$  for a 1-cm<sup>2</sup> chip with  $F = 100$  nm, so even with an aggressive  $M = 100$ , the total number of wasted crosspoint devices is  $<5\%$ .

## Discussion

Four labels (i.e., the row and column addresses for each of the two via types in the CMOS area interface) are required to specify the address of each crosspoint device, thus mapping the three-dimensional device location to a four-dimensional address space. The physical device location is specified by the spatial position of the line fragment in the Euclidean space and its relative position inside the fragment.

In Fig. 3, all of the wire and via patterns are identical in all of the crossbar layers. Consequently, the area density of the vias is kept constant through all of the stacked layers, and adding new layers does not require any changes in the layers below. Thus, this scheme for stacking crossbar layers can be very cost efficient, requiring only a few unique sets of patterning masks or molds if features are defined by optical photolithography or nanoimprint technology, respectively. At the same time, the via density of the area interface can be high enough such that the communication throughput is also very high.

Unlike the original CMOL concept (11), stacking of multiple crossbars would require layer-to-layer alignment in positioning wires and vias. For state-of-the-art photolithography, the overlay accuracy (i.e.,  $3\sigma$ , where  $\sigma$  is the standard deviation) is typically at least five times smaller than the minimum feature size  $F$  (2).<sup>‡</sup> Moreover, only the relative alignment between the adjacent patterned layers is important, so the overlay alignment error does not accumulate with stacking. For example, Fig. 4 illustrates one plausible way of sustaining the minimum feature size of patterning technology as the number of layers grows by replicating the alignment mark at each step. The features at every patterning step are produced only at that level (i.e., there is no

<sup>‡</sup>The overlay accuracy for nanoimprint technology is not as good as that of the state-of-the-art photolithography yet. For example, the best commercially available tool for nanoimprint, Imprio300 (23), offers patterning of sub-32-nm features with  $\approx 10$ -nm overlay accuracy across a single wafer. Nevertheless, expectations that overlay accuracy for this relatively immature technology will improve rapidly are realistic.

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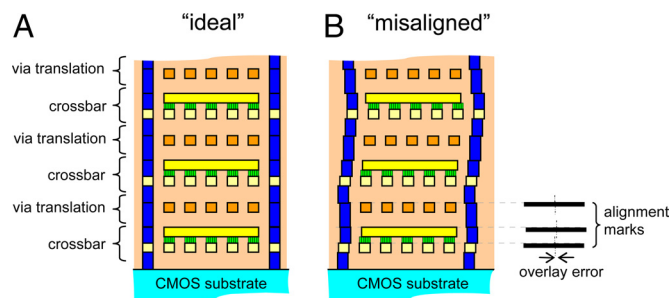


Fig. 4. Cross-section of three-dimensional circuit illustrating (A) “ideal” alignment between layers and (B) more realistic scenario with overlay error.

requirement to etch through to lower levels). For many contemporary CMOS circuits, the size of the metal wires typically becomes larger with each succeeding layer, but this is not a fundamental requirement. Rather, it is a convenient feature resulting from the fact that wires in higher layers of an integrated circuit interconnect stack usually are required to conduct larger currents than those in lower layers and the use of a lower-resolution lithography tool for the higher metal layers to lower production costs. For a sufficiently valuable chip, the same quality of surface polish and photolithography can be applied to multiple levels.

The combination of high bandwidth and density can be used effectively for various applications besides digital stand-alone memories. For example, memristive devices can act as programmable connections in a hybrid FPGA circuit (19, 24, 25) and as electronic versions of synapses in bio-inspired adaptive networks (20, 26, 27). For these applications, the most important characteristics of the circuit architecture are the programmable complexity (or crosspoint device density) and connectivity of the cells. With the area interface, any CMOS cell can be connected directly to  $M\beta^2$  other cells through a single memristive device. Over the long term, we see that this stacking technology offers the possibility of continued scaling of memory density (e.g., for  $M = 100$  and  $F = 10$  nm the theoretical density is as high as 100 terabits per square centimeter). This would be equivalent to the result of another 15 years of Moore’s Law memory scaling for which lateral shrinkage is replaced by stacking.

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