
Monolithic Incorporation of III-V in Silicon for I/O and Digital Logic

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Semiconductor Trends

- Silicon manufacturing morphing to new semiconductor materials
 - Core digital silicon rapidly out-performing ability to use computing capability
 - Core digital silicon employing SiGe for strained silicon
 - R&D shows higher Ge concentrations necessary for continued low power high performance computation
 - Serious investments in understanding III-V role in future
- III-V manufacturing static in comparison
 - Plenty of performance
 - Markets for III-V-only well-known
 - III-V logic in III-V infrastructure will not happen for high transistor counts

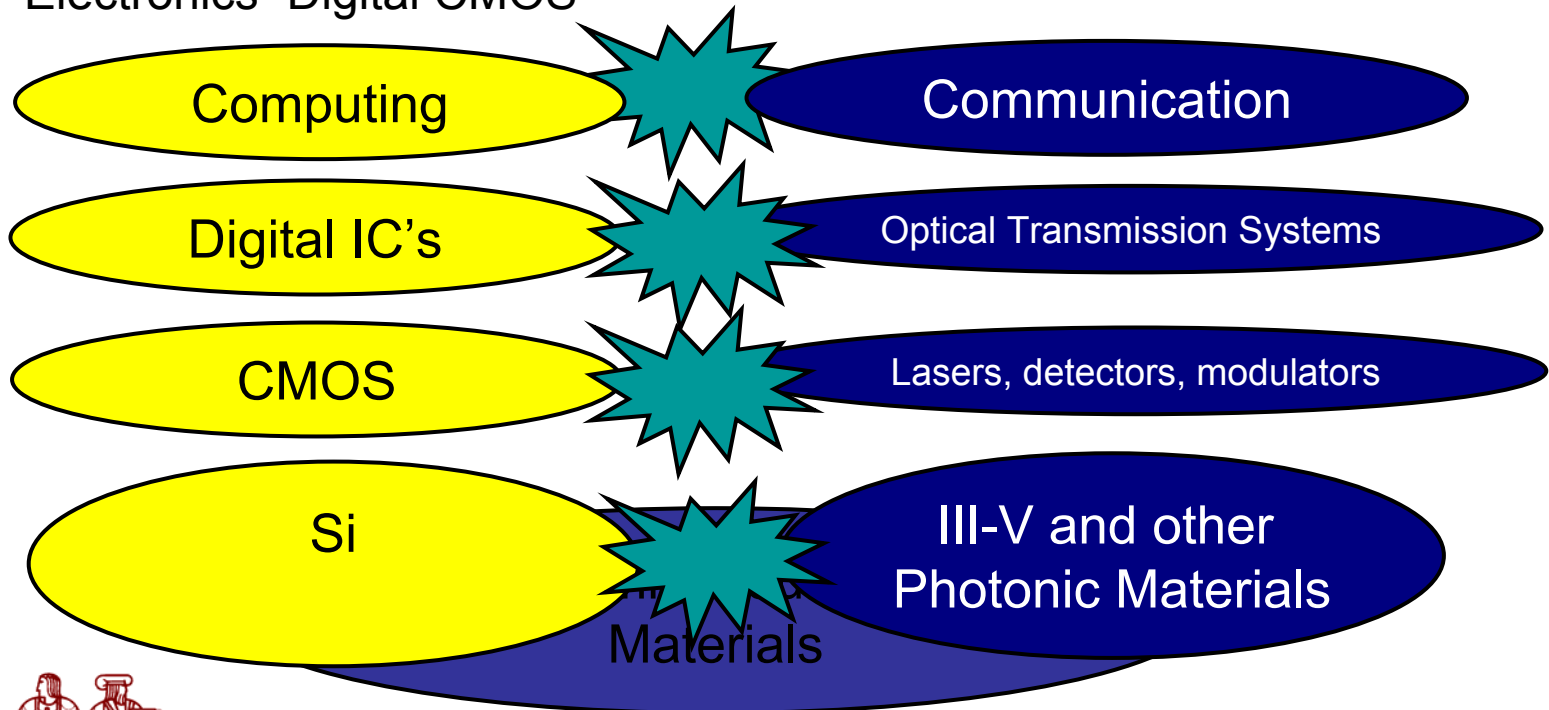
Market, Technology, and Manufacturing Trends
Support III-V Monolithic Integration with Silicon

Timeline won't keep CEO's up late at night- YET

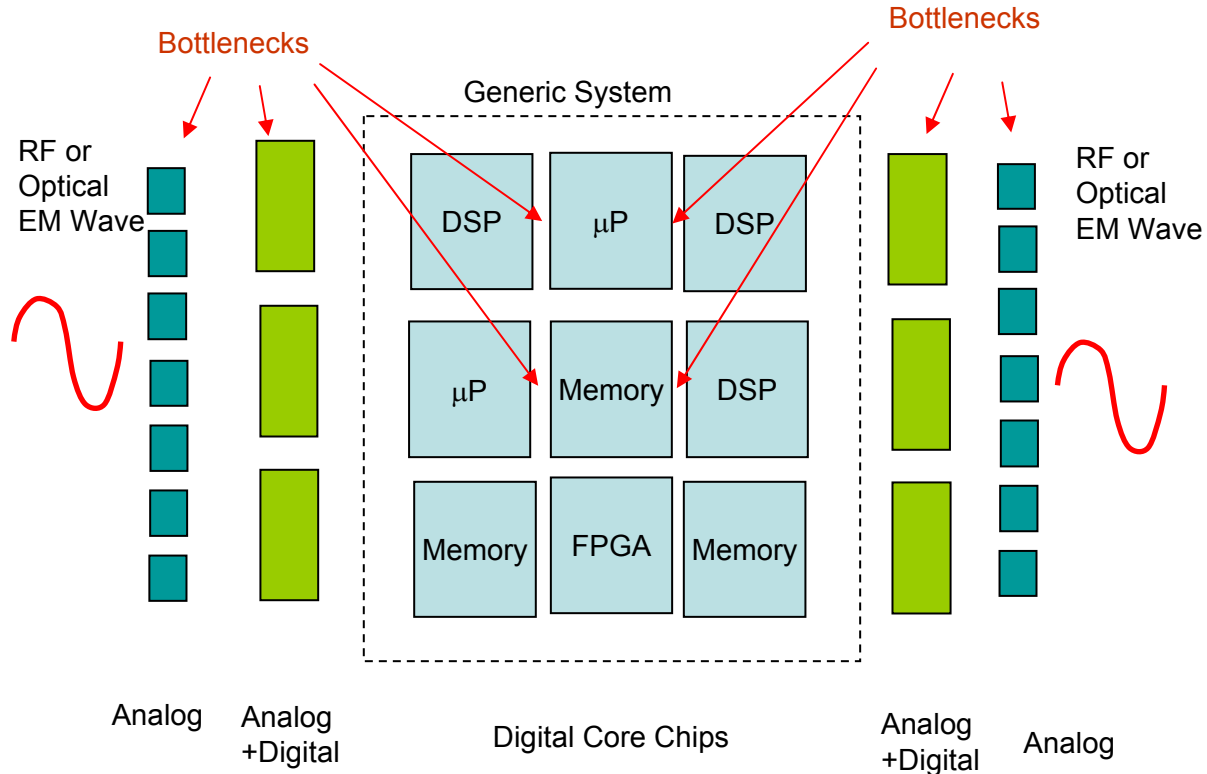


Limits in Electronic/Photonic Systems begin at Fundamental Materials Level

- Materials selections for photonics and electronics occurred ~30-40 years ago
- Supply/Value chains developed separately
 - Photonics=Telecom
 - Electronics=Digital CMOS

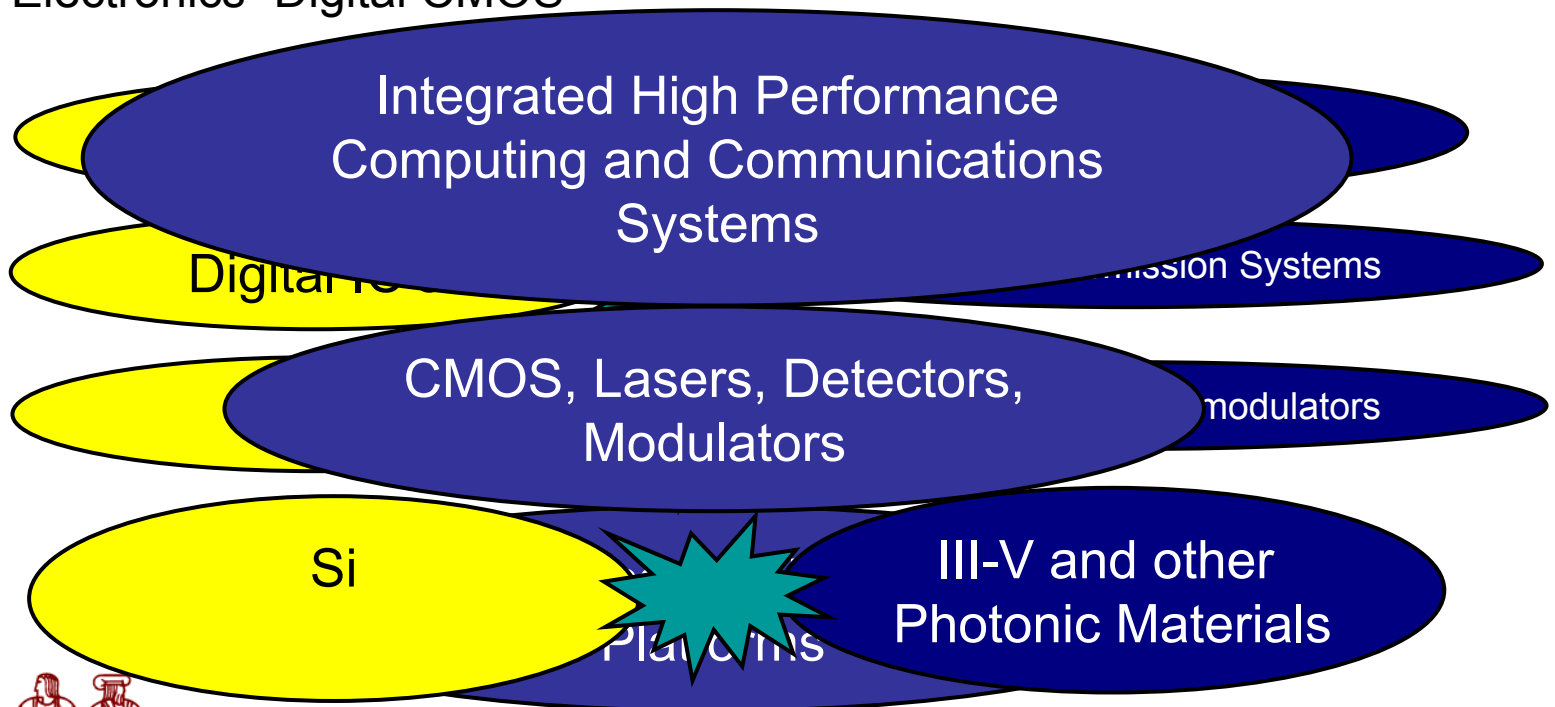


The Need for New CMOS-compatible Materials Platforms

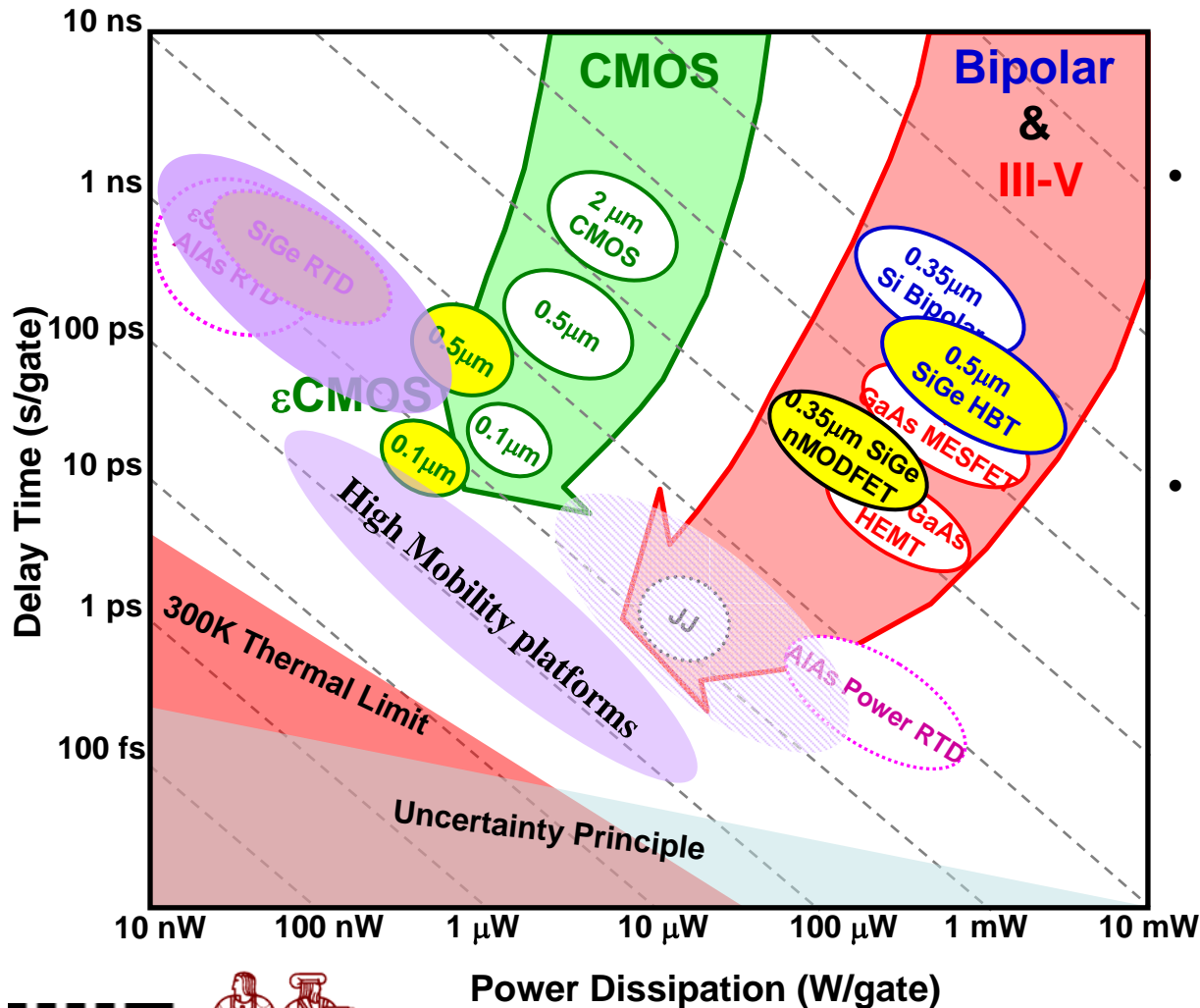


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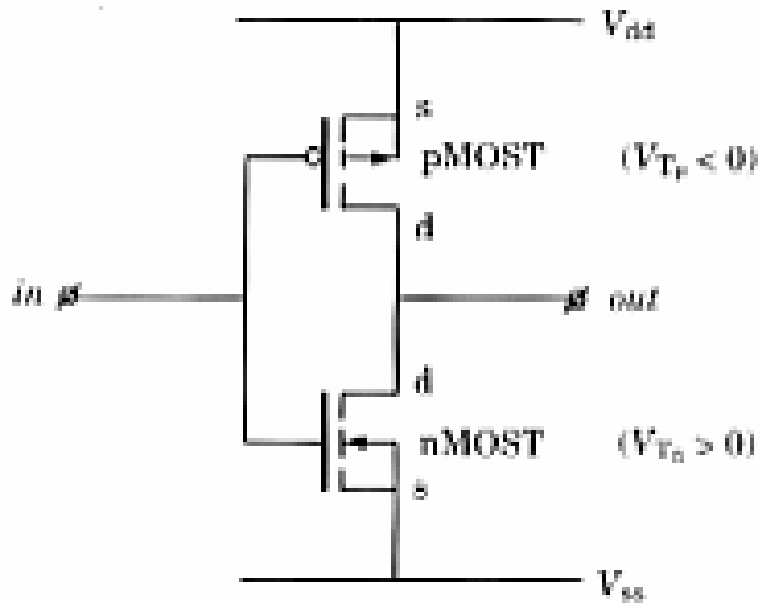
Power-Delay Product



- Power-delay depends on
 - Architecture
 - Circuits
 - Devices **scaling=>process**
 - **Materials**
- High mobility materials deliver lower power-delay product at the material/substrate level!

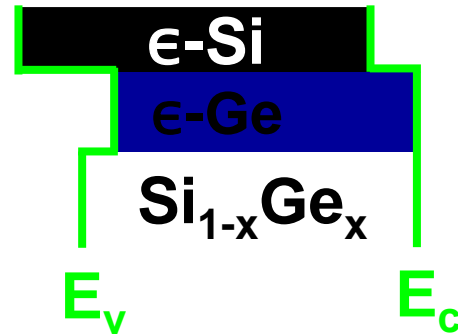
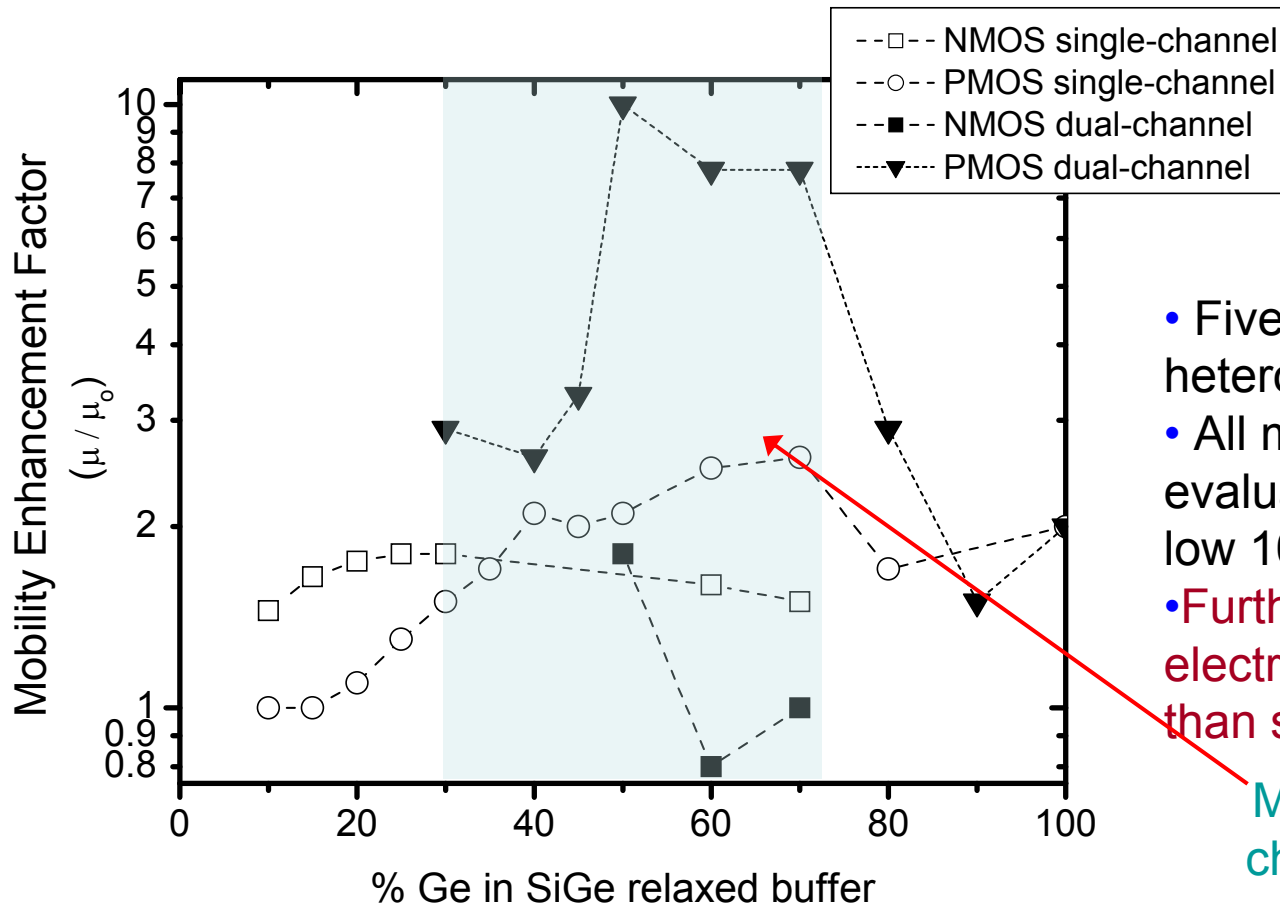


New Channel Materials: NMOS AND PMOS



- Low field mobility remains a factor
- Maximum IV-based μ_e in ϵSi $\sim 2x$
- Maximum IV-based μ_h in ϵGe $\sim 10x$

Column IV mobility potential



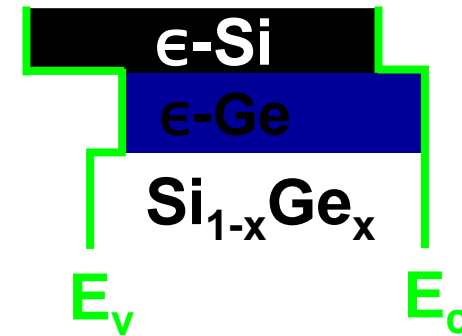
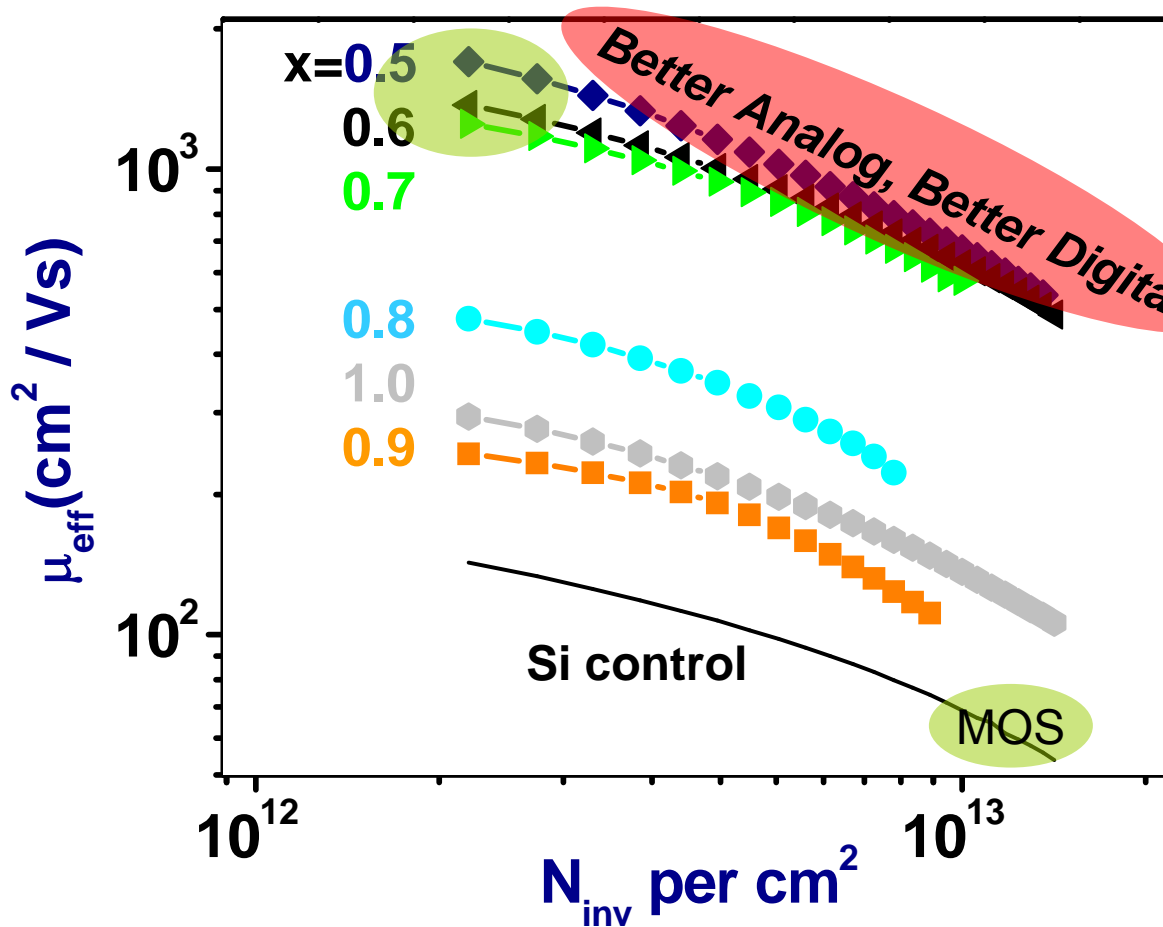
- Five years of mapping SiGe heterostructures
- All mobility enhancements evaluated at $N_{inv} \sim$ high 10^{12} to low 10^{13} cm^{-2}
- Further increases will require electron enhancement greater than strained Si \rightarrow III-V

Most interesting region challenges device layer critical thickness



μ_{eff} in ϵ -Si/ ϵ -Ge p-MOSFETs

III-V HEMTs

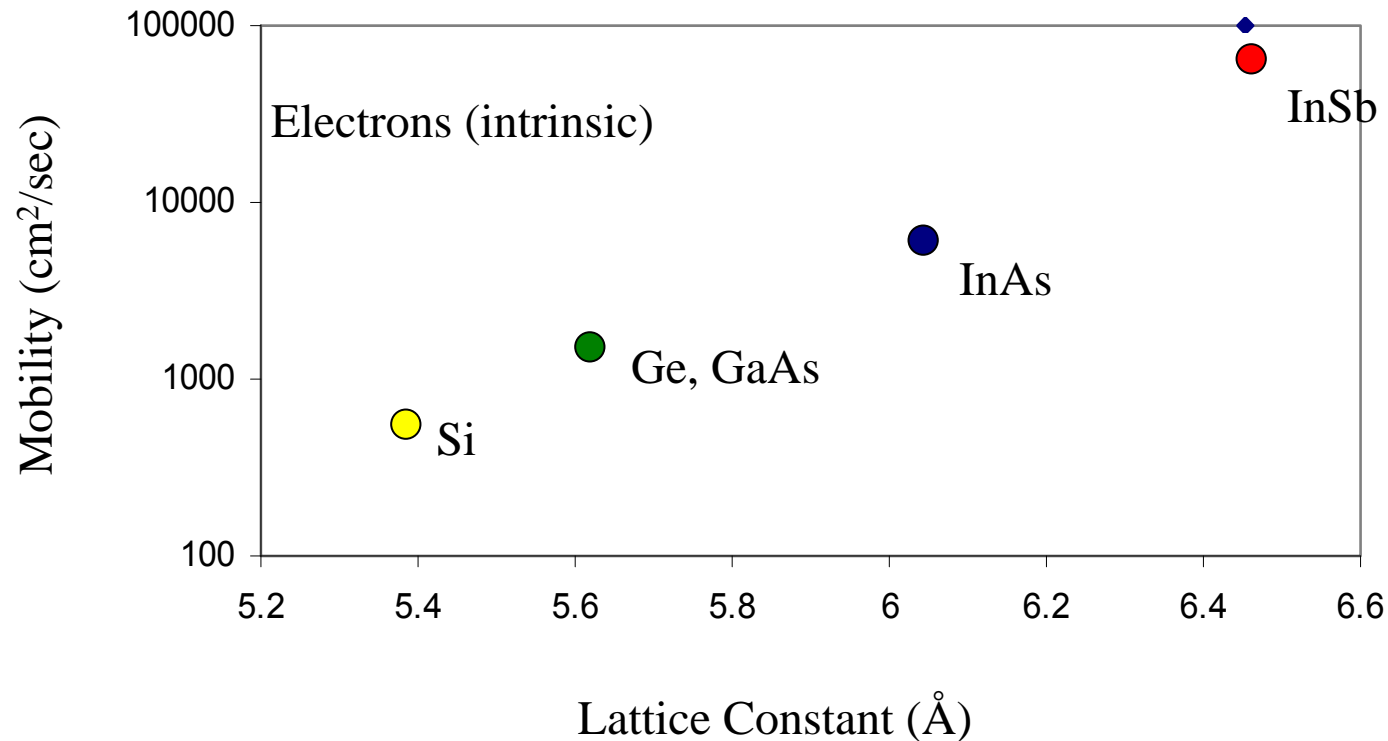


- Higher strain leads to higher μ_{eff}
 - Decreased in-plane m^* , LH-HH scattering



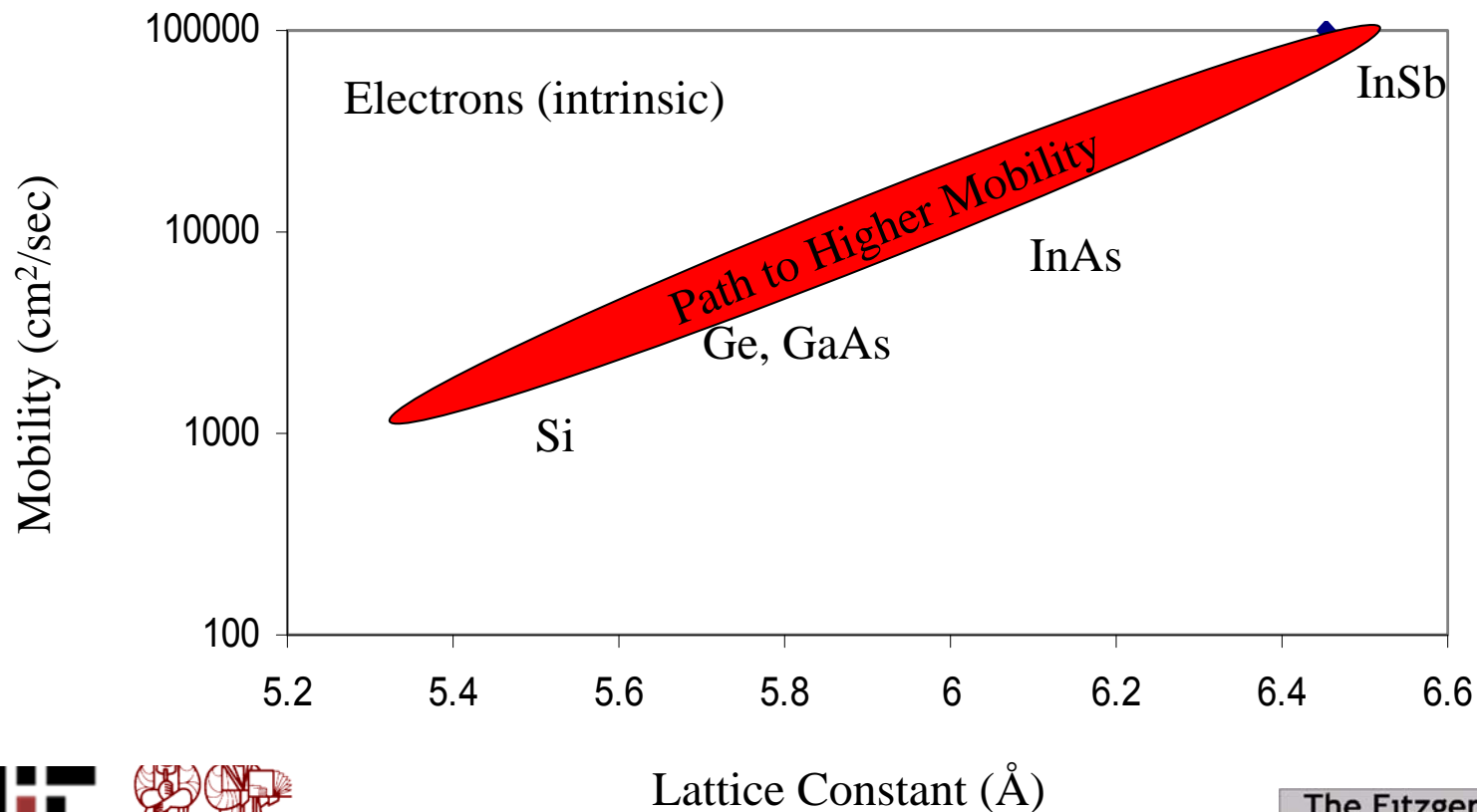
Mobility Trends with Semiconductor Lattice

- Periodic Table creates unavoidable relation between lattice and carrier mobility, through effective mass
- Straining lattice is a way to influence carrier mobility for a given lattice, influence through both m^* and τ
- Limit on ability to strain about a given lattice is limited by plastic relaxation



Mobility Trends with Semiconductor Lattice

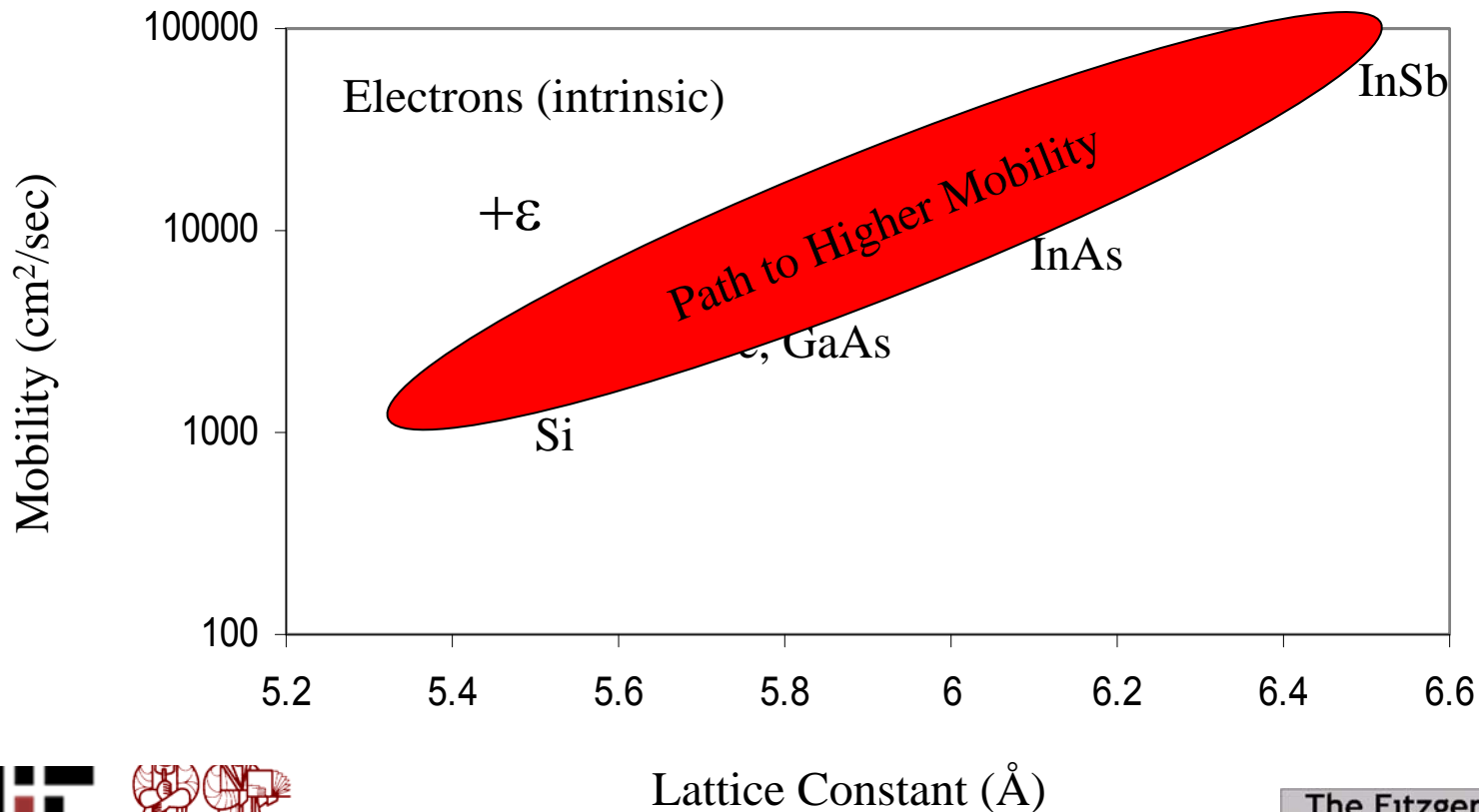
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Lattice Constant (\AA)

Mobility Trends with Semiconductor Lattice

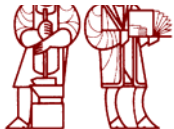
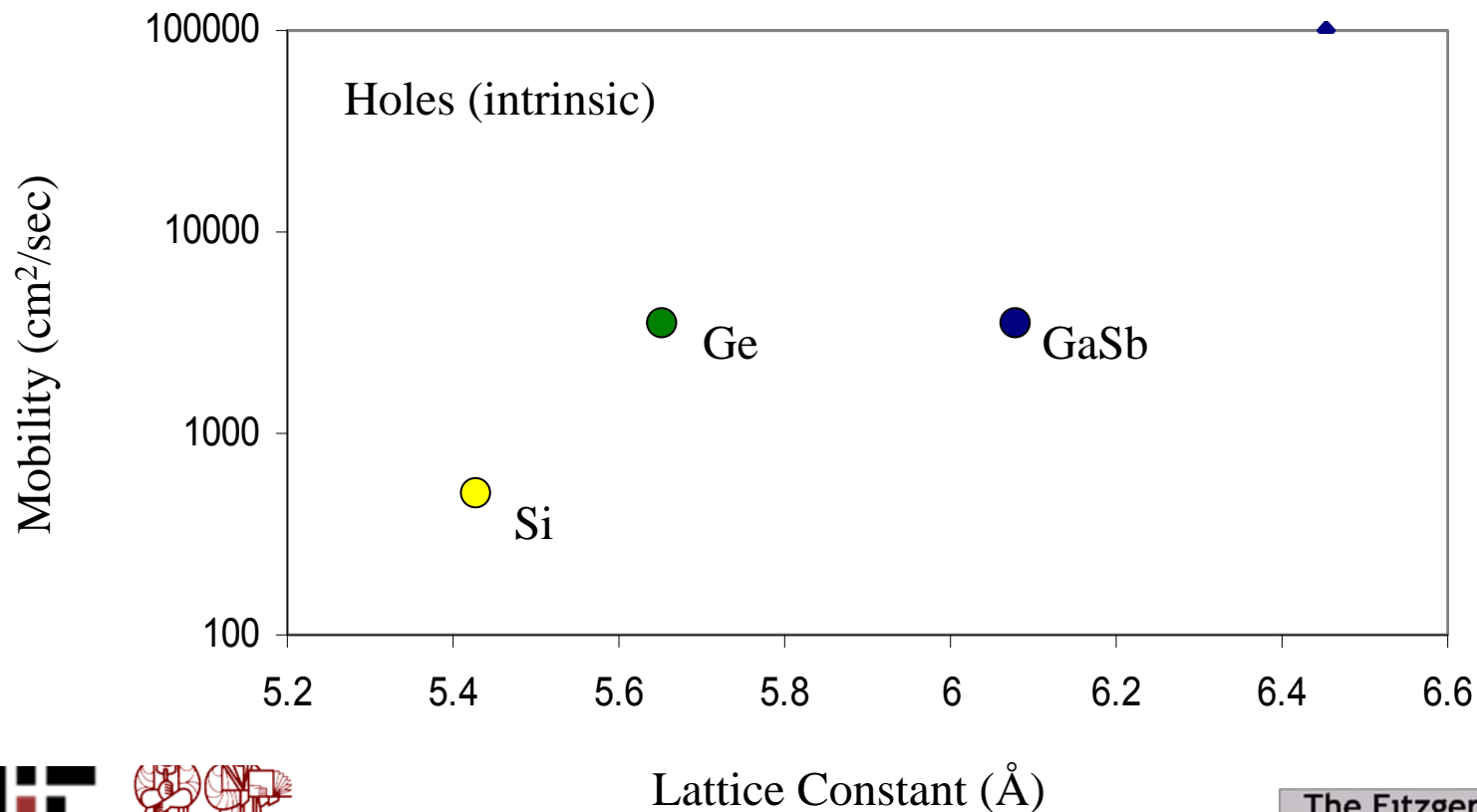
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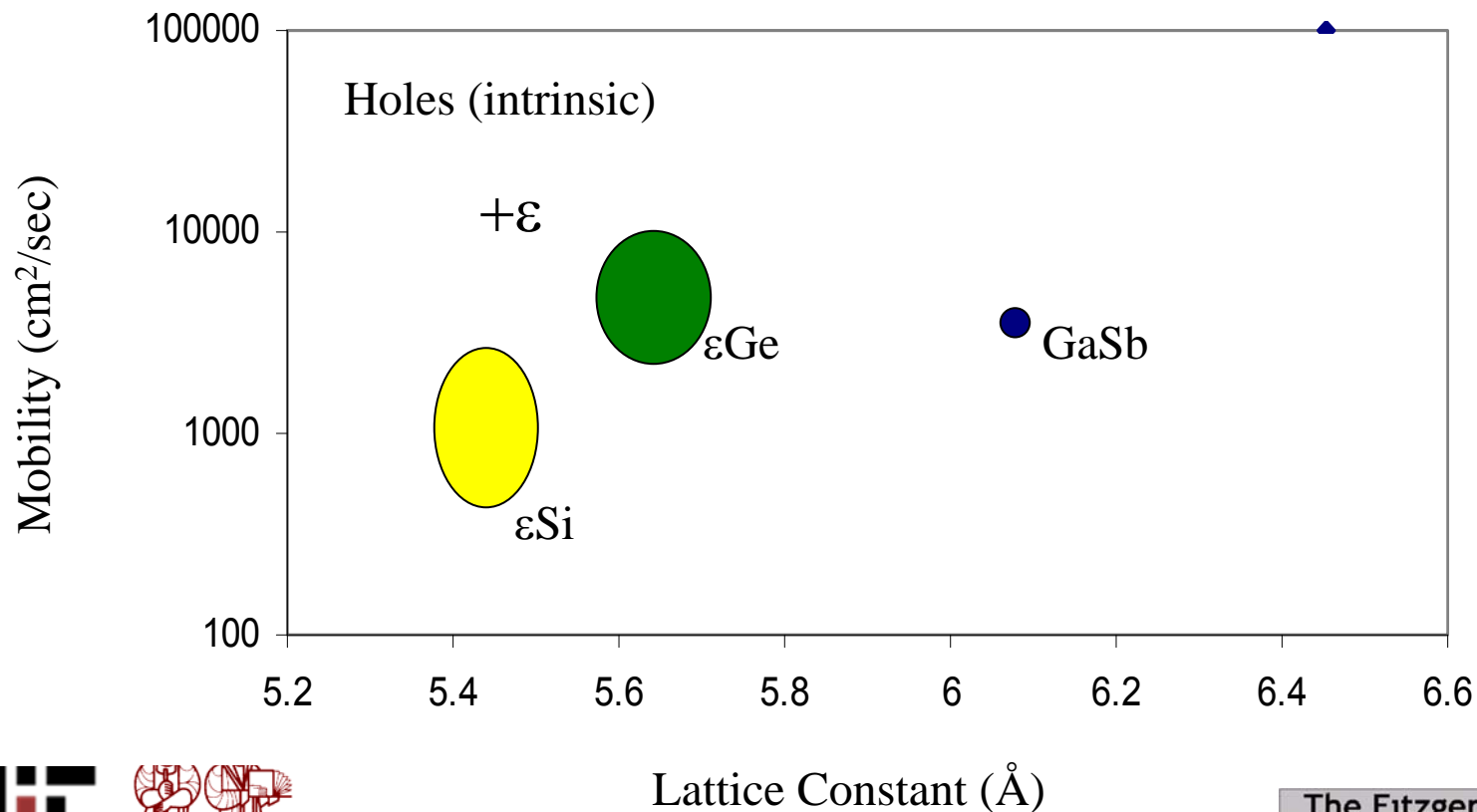
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Lattice Constant (Å)

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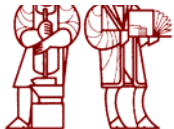
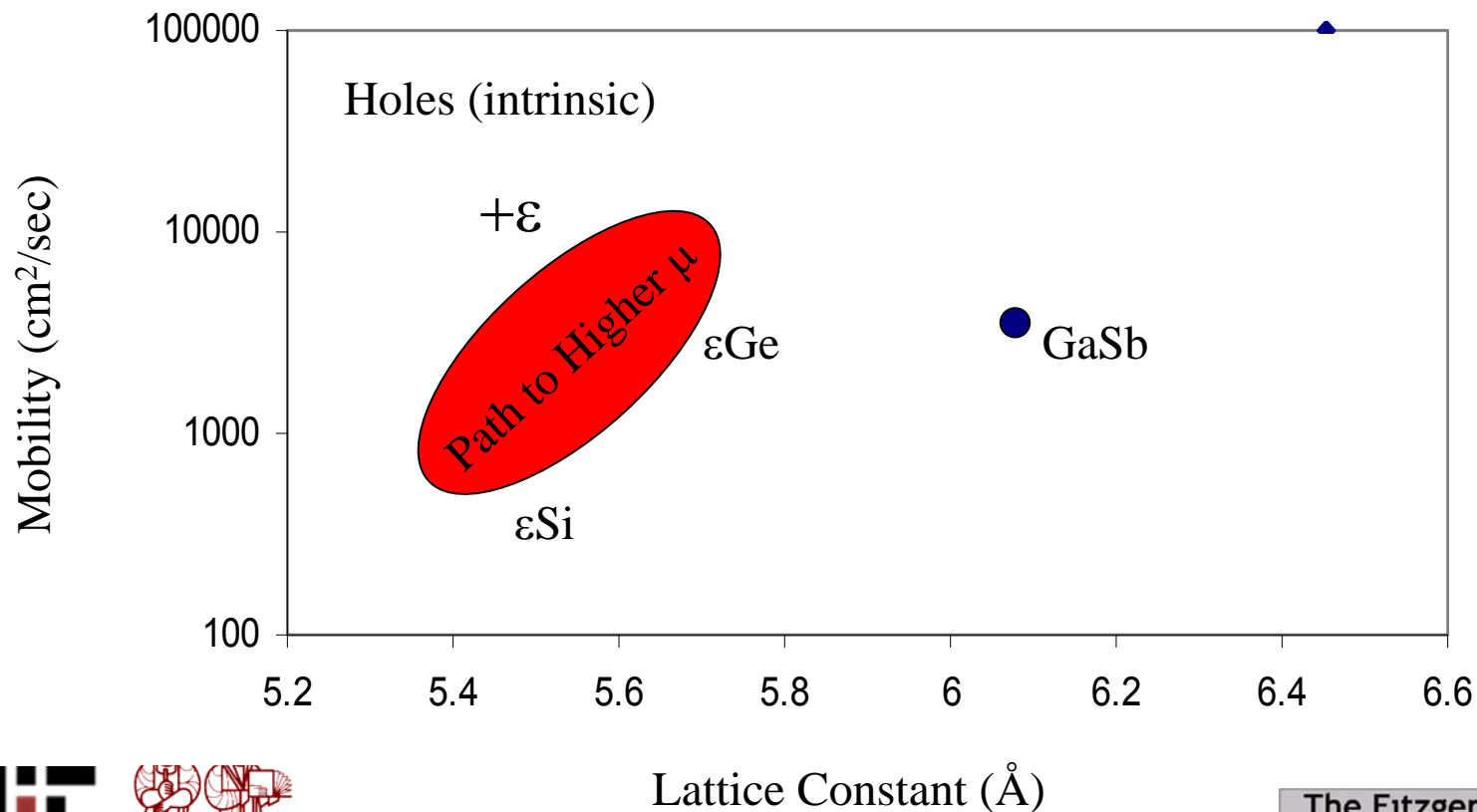
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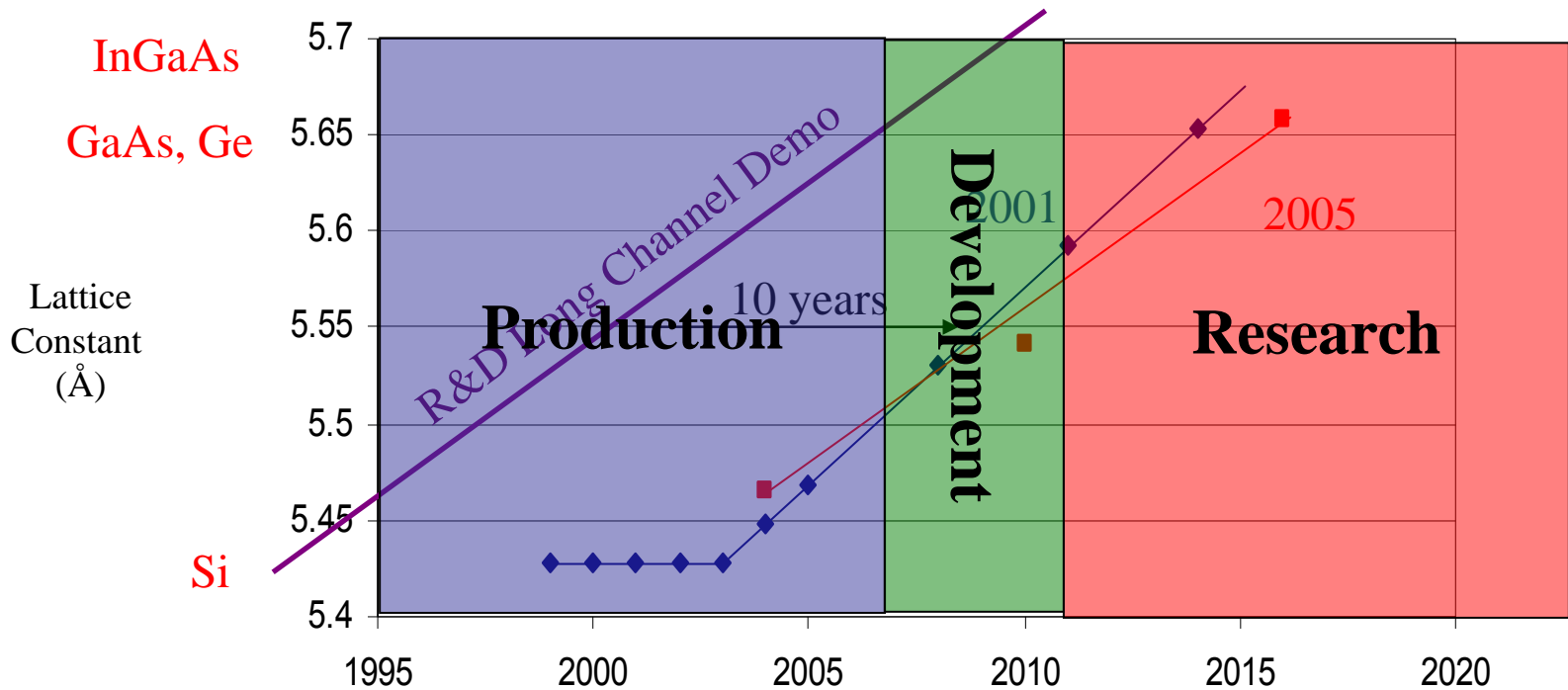
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Lattice Constant (\AA)

Lattice Constant Roadmap

- Original 2001 prediction and 2005



Year

Trends Conclusion

- Digital CMOS trends headed toward Ge/III-V lattice on Si
 - → from digital core out
- Will there be a trend from III-V analog/optical *inward* toward digital core?
- **If so, which one is faster?**



Our III-V/Si Roadmap

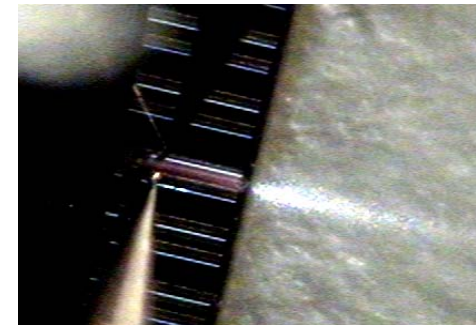
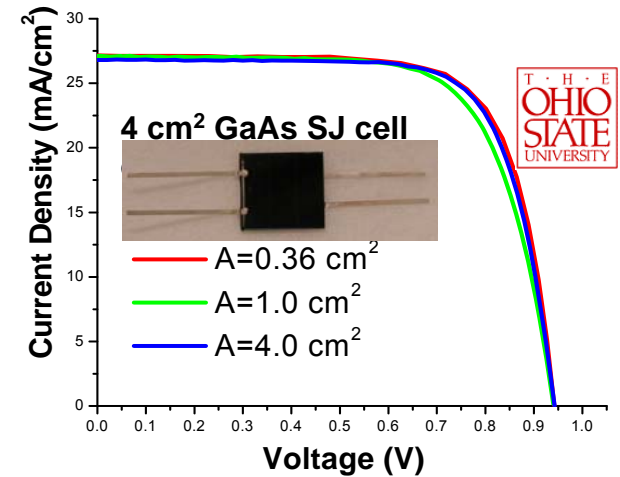
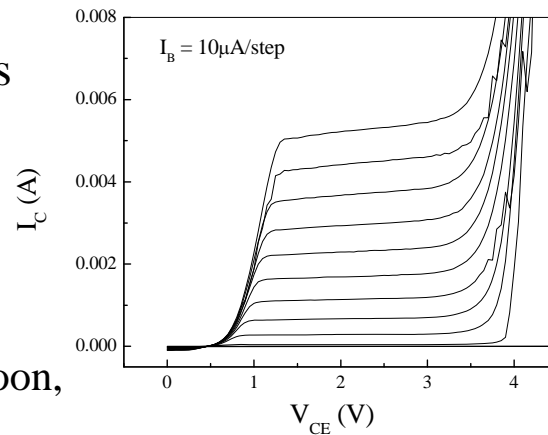
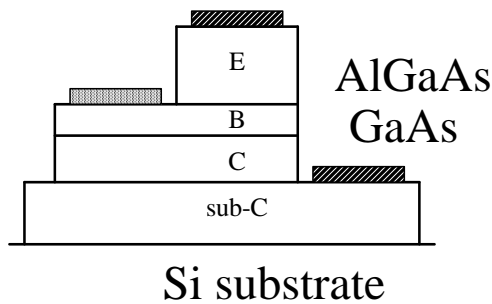
- Materials Platforms
 - Substrate materials capable of supporting III-V devices on silicon
- Application Areas
 - III-V + Si CMOS (analog/optics inward)
 - Process integration and epi supporting processing of III-V devices in silicon fabrication environments
 - III-V MISFET (digital core outward)
 - In-situ basic studies of interface structure/electronic properties correlation
- Commercialization
 - Driver markets benefiting from combination of non-leading-edge CMOS and known III-V devices
- **Due to the possibility of many smaller higher growth markets, III-V incorporation from communication interface inward to digital core is likely faster**



Research Device Prototypes

Proving Material Quality exist for III-V/Si

- Solar Cells
- Primitive Monolithic Links
- CW RT Lasers
- GaAs-based HBTs



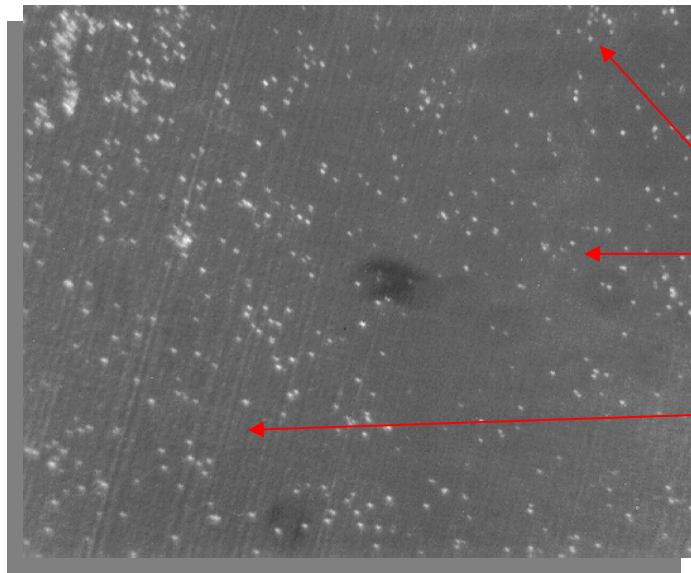
In collaboration with Prof. Yoon,
NTU, Singapore



Relaxed Compositionally Graded $\text{Si}_{1-x}\text{Ge}_x$ Buffers

- Introduce lattice-mismatch in small increments
- Less threading dislocations required to relax strain
- Overall grading rate: 10% Ge/ μm
- Fully relaxed 100% Ge cap
- TDD: less than 10^6 cm^{-2}

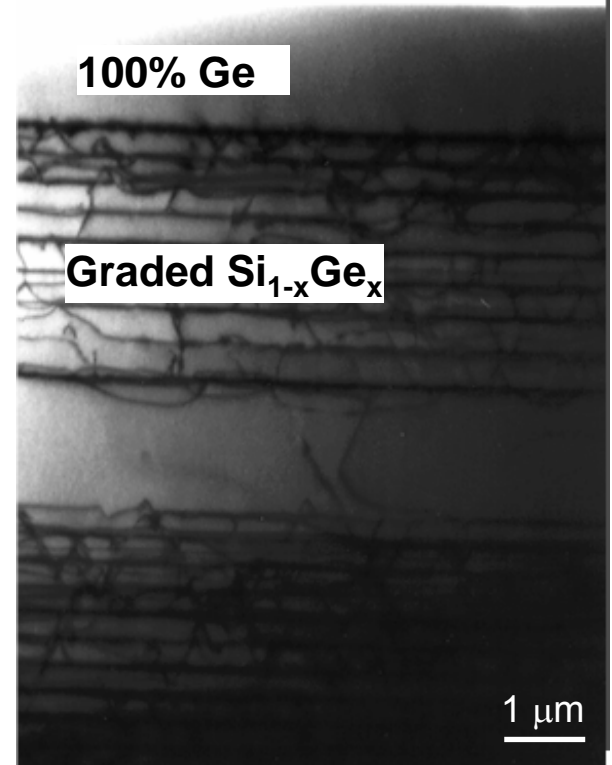
Plan-view Nomarski image



Dislocation etch pits

“Crosshatch”
surface roughness

RMS = 24.2nm



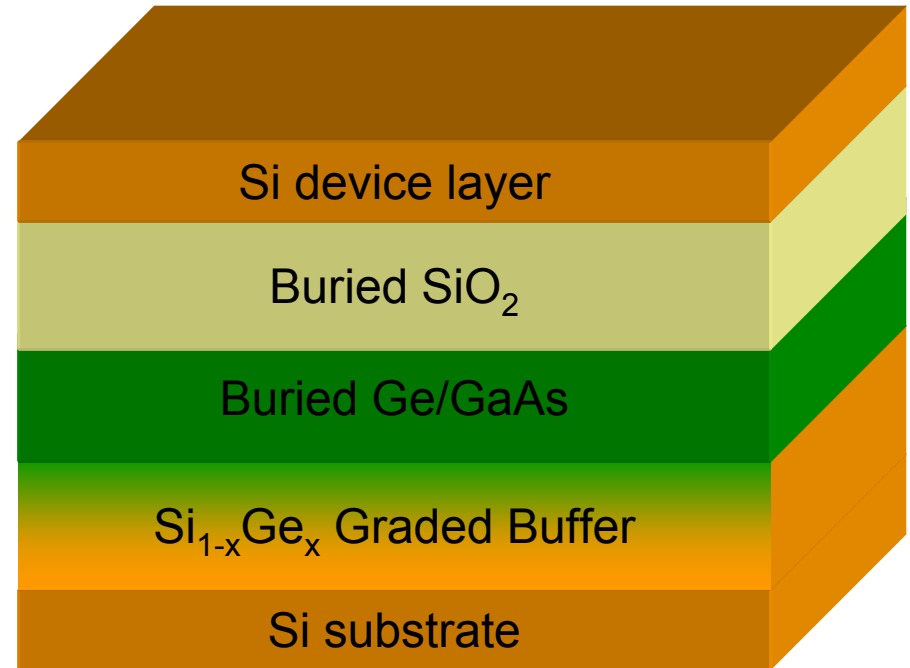
Cross-sectional TEM image

- M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz and E. A. Fitzgerald, *Appl. Phys. Lett.* **72** (14), 1718 (1998).



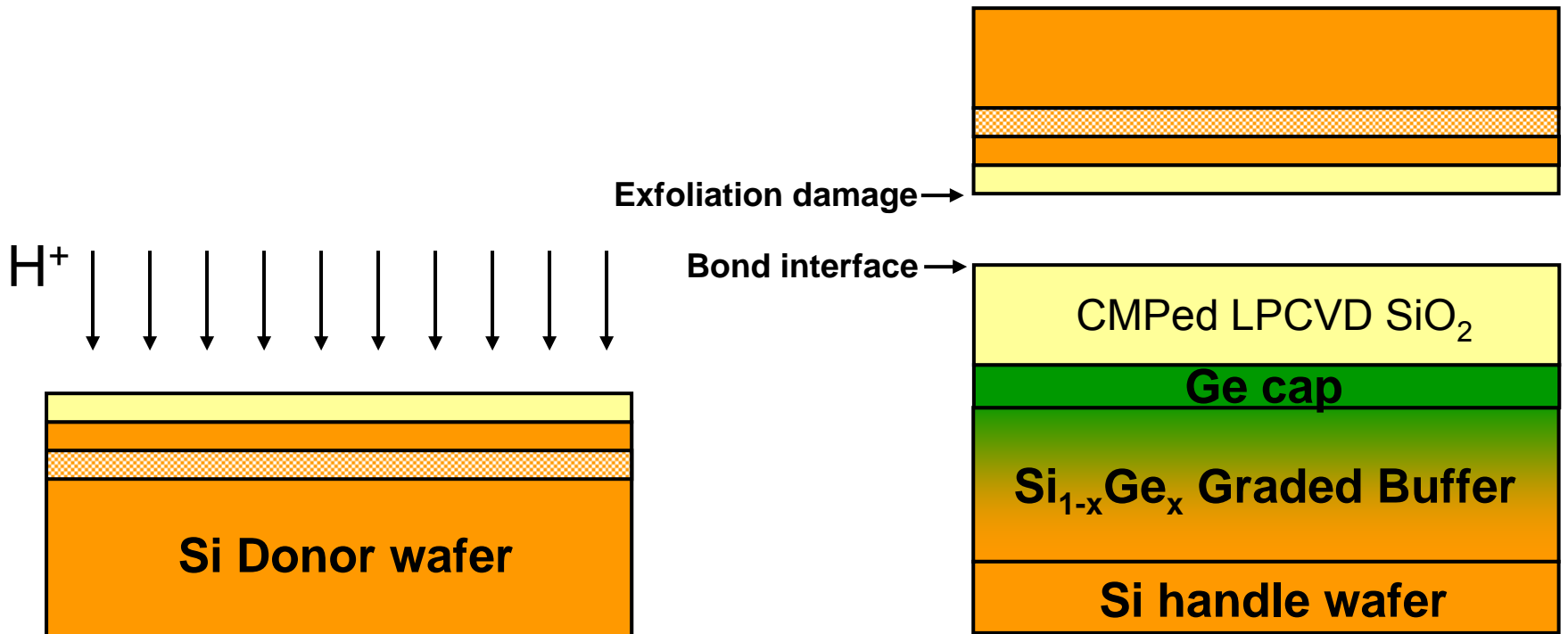
Silicon on Lattice-Engineered Substrate (SOLES)

- SOLES is a platform for coplanar integration
- By burying the GaAs layer, this wafer can be processed similarly to a standard SOI wafer
- After CMOS processing, GaAs device layer can be accessed by etching through Si device layer and buried SiO₂ layer
- Can be fabricated using standard semiconductor processing



Basic SOLES Process Overview

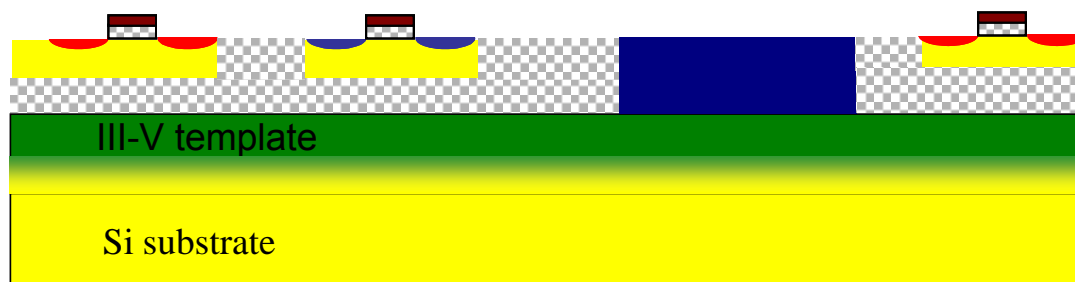
- Starting Materials: Si donor wafer, Si handle wafer with graded buffer



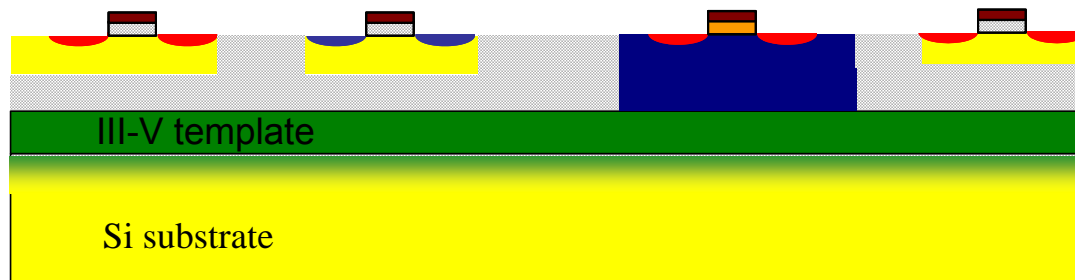
Front-end CMOS
Fabrication



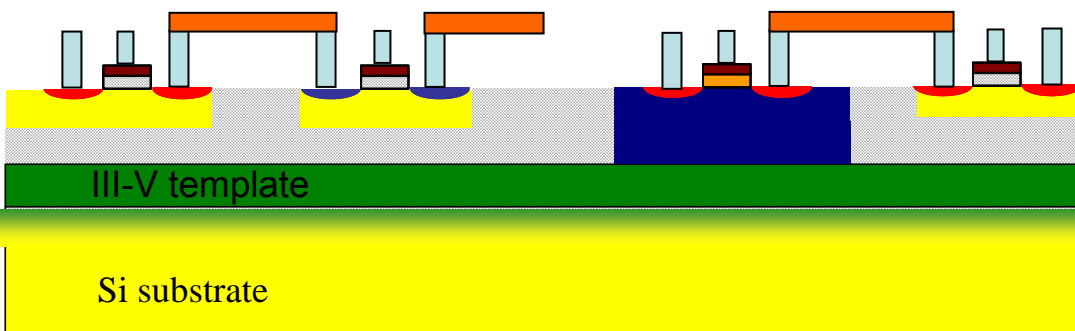
III-V Device Layer Growth



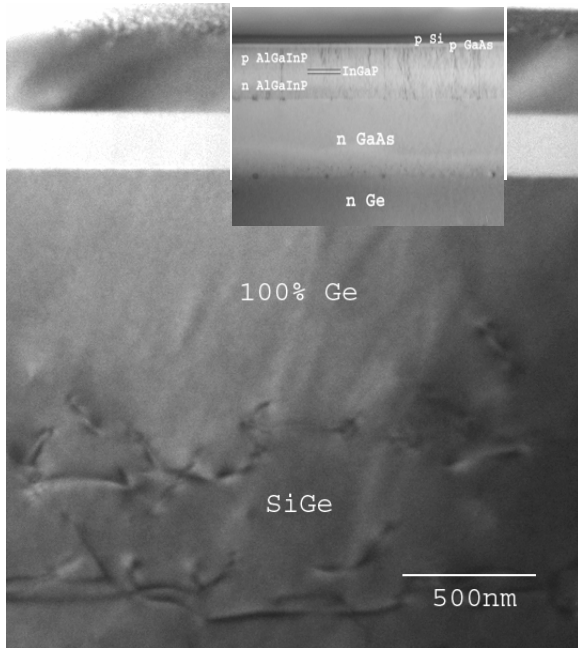
III-V Device Layer
Fabrication



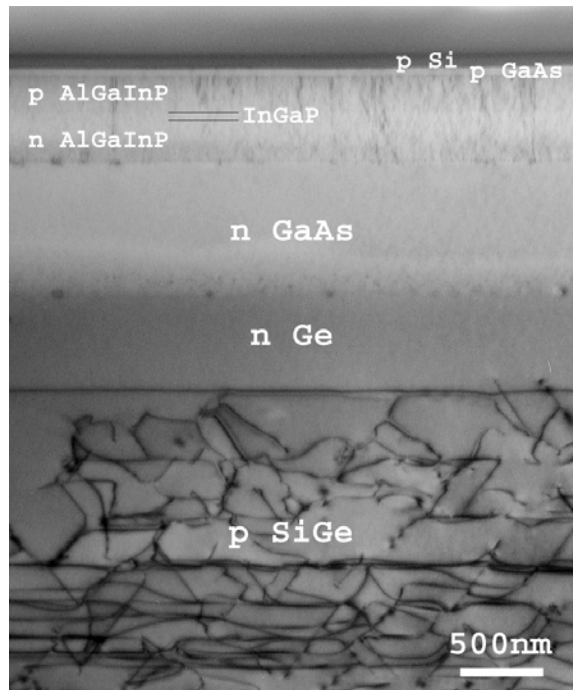
Silicon IC Back-end
Processing
(inter-level dielectric
not shown)



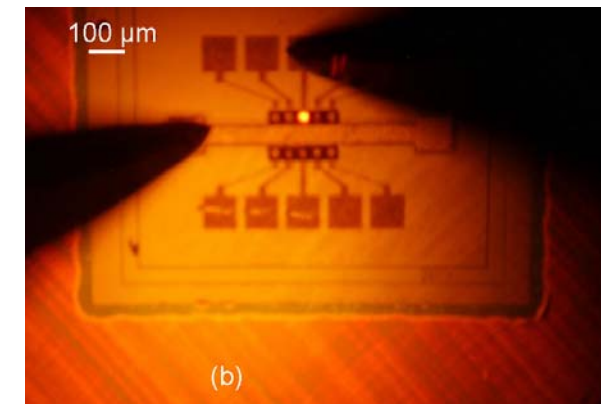
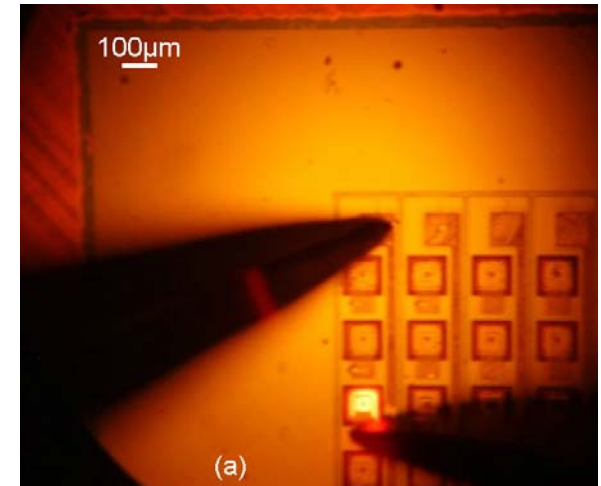
Monolithic Visible LED Arrays on Si using SOLES and CMOS-compatible processing



Silicon On Lattice-Engineered Silicon (SOLES)



III-V Device Epi

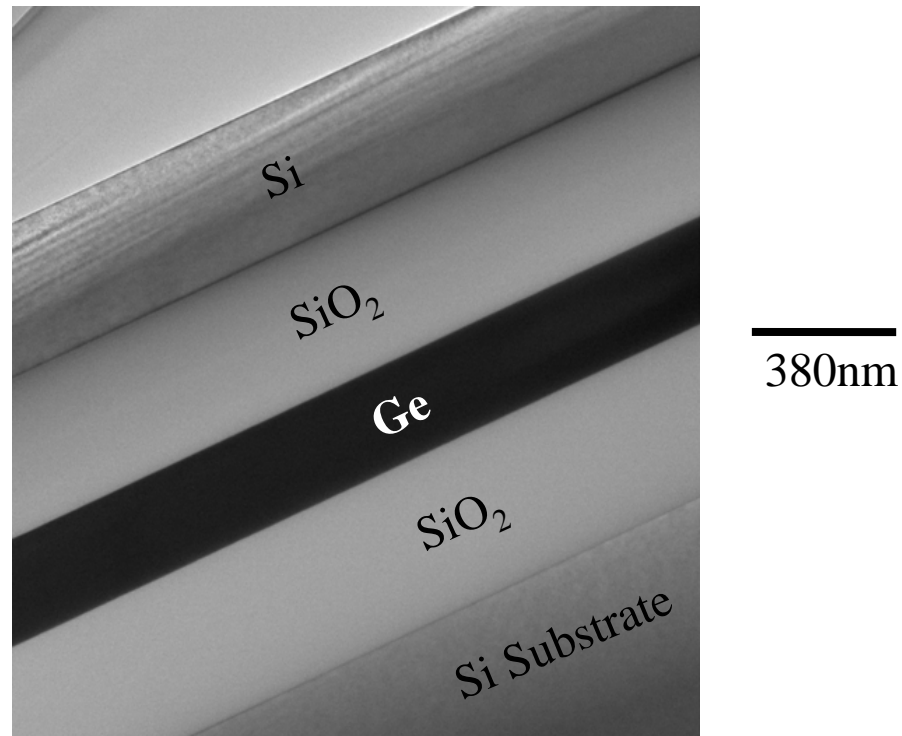


Silicon-like processing



Double Smart-cut Based SOLES

- Smart-cut Ge template followed by conventional Smart-cut

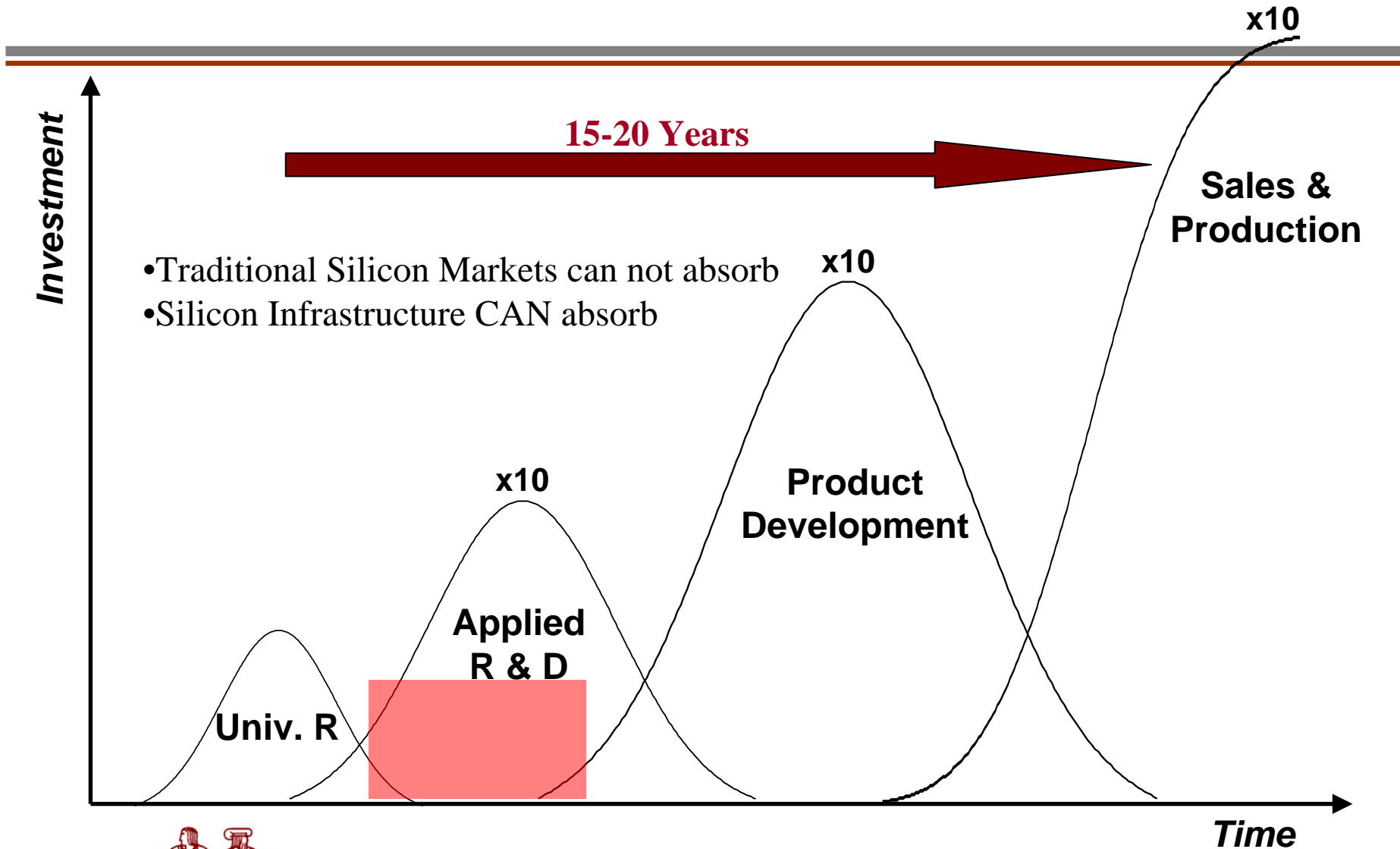


Why Monolithic III-V/Si has More Value than most Hyped Technologies

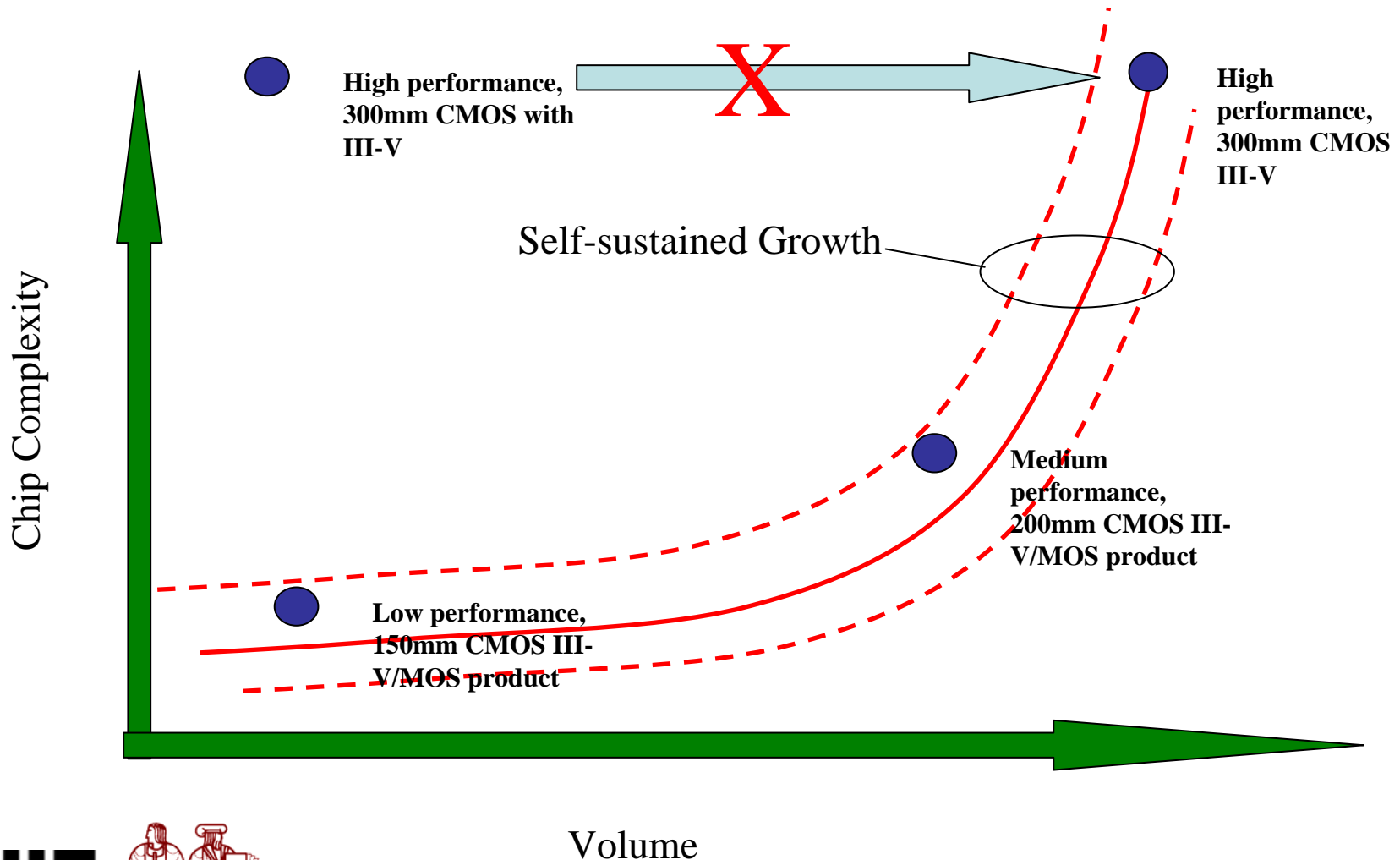
- Markets, Technology, Implementation
 - Markets
 - *Many*: III-V electronics and photonics bring fundamentally new utility to silicon systems (for core CMOS, much later)
 - Technology
 - Last 20 years have *removed* fundamental barriers
 - **MORE** R&D required to move across the university/commercial boundary (but trying to make silicon lase, for example, is a waste of resources)
 - Implementation
 - *Compatible* with Silicon manufacturing technology
 - Intersection with **target markets** and **manufacturing** necessary to
 - innovate
 - **define** research and development
 - move technology forward



From Research to Production



Path for III-V/Si: Untraditional Smaller Markets



Summary

- Monolithic III-V+Si IC's
 - Potentially 5 years to small volume IC's, 10 years to multiple market access and thriving companies (small and medium)
 - Current needs
 - Increased R&D supporting substrates and materials that have shown promise
 - Device and Circuit research in context of most promising markets (needs materials etc.)
 - Identify first commercial widgets within 3-5 years
 - Drives material supply, process knowledge, and expertise
 - Long-term migration of commodity III-V devices to silicon manufacturing infrastructure
- Monolithic III-V MISFET for logic
 - Basic research required with in-situ control of ideal systems
 - Process integration research to optimize MISFETs follows
 - Research dovetails with nascent industry produced from III-V+ Si IC's



Acknowledgements

- Funding
 - Army Research Office, John Prater
 - Singapore-MIT Alliance
 - MARCO IFC, MSD
- Collaborations
 - SOITEC
 - Double Smart-cut SOLES

