

# Macroelectronics: Perspectives on Technology and Applications

ROBERT H. REUSS, SENIOR MEMBER, IEEE, BABU R. CHALAMALA, SENIOR MEMBER, IEEE, ALINA MOUSSESIAN, MEMBER, IEEE, MICHAEL G. KANE, AMRITA KUMAR, DAVID C. ZHANG, JOHN A. ROGERS, MILTOS HATALIS, SENIOR MEMBER, IEEE, DOROTA TEMPLE, GARRET MODDEL, BLAKE J. ELIASSON, MICHAEL J. ESTES, JOSEPH KUNZE, ERIK S. HANDY, ERIC S. HARMON, DAVID B. SALZMAN, JERRY M. WOODALL, FELLOW, IEEE, M. ASHRAF ALAM, JAYATHI Y. MURTHY, STEPHEN C. JACOBSEN, MARC OLIVIER, DAVID MARKUS, PAUL M. CAMPBELL, AND ERIC SNOW

## Invited Paper

Manuscript received January 13, 2005; revised April 4, 2005.

R. H. Reuss is with the Defense Advanced Research Projects Agency Microsystems Technology Office (DARPA/MTO), Arlington, VA 22203 USA (e-mail: robert.reuss@darpa.mil).

B. R. Chalamala is with Indocel Technologies, Research Triangle Park, NC 27709-2238 USA (e-mail: chalamala@indocel.net).

A. Moussessian is with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA (e-mail: alina.moussessian@jpl.nasa.gov).

M. G. Kane is with Sarnoff, Princeton, NJ 08540 USA (e-mail: mkane@sarnoff.com).

A. Kumar and D. C. Zhang are with Acellent Technologies, Inc., Sunnyvale, CA 94089 USA (e-mail: akumar@acellent.com; zhang@acellent.com).

J. A. Rogers is with the University of Illinois, Urbana, IL 61801 USA (e-mail: jrogers@uiuc.edu).

M. Hatalis is with Lehigh University, Bethlehem, PA 18015-3193 USA (e-mail: mkh1@lehigh.edu).

D. Temple is with RTI International, Research Triangle Park, NC 27709-2889 USA (e-mail: temple@rti.org).

G. Moddel is with the Phiar Corporation, Boulder, CO 80302 USA, on leave from the University of Colorado, Boulder, CO 80309-0425 USA (e-mail: moddel@phiar.com).

B. J. Eliasson is with the Phiar Corporation, Boulder, CO 80302 USA (e-mail: eliasson@ieee.org).

M. J. Estes is with Melles Griot Electro-Optics, Longmont, CO 80503 USA (e-mail: mestes@carlsbad.mellesgriot.com).

J. Kunze and E. S. Handy are with SI2 Technologies, Inc., Chelmsford, MA 01824 USA (e-mail: jkunze@si2technologies.com; chandy@si2technologies.com).

E. S. Harmon is with LightSpin Technologies, Inc., Norfolk, MA 02056 USA (e-mail: harmon@lightspintech.com).

D. B. Salzman is with LightSpin Technologies, Inc., Bethesda, MD 20824-0198 USA (e-mail: salzman@lightspintech.com).

J. M. Woodall and M. Ashraf Alam are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907-2035 USA (e-mail: woodall@ecn.purdue.edu; alam@ecn.purdue.edu).

J. Murthy is with the School of Mechanical Engineering, Purdue University, West Lafayette, IN 47907-2088 USA (e-mail: jmurthy@purdue.edu).

S. C. Jacobsen, M. Olivier and D. Markus are with Sarcos, Salt Lake City, UT 84108 USA (e-mail: jacobsen@sarcos.com; m.olivier@sarcos.com; d.markus@sarcos.com).

P. M. Campbell and E. Snow are with the Naval Research Laboratory, Washington, DC 20375-5000 USA (e-mail: campbell@bloch.nrl.navy.mil; snow@bloch.nrl.navy.mil).

Digital Object Identifier 10.1109/JPROC.2005.851237

*Flexible, large area electronics—macroelectronics—using amorphous silicon, low-temperature polysilicon, or various organic and inorganic nanocrystalline semiconductor materials is beginning to show great promise. While much of the activity in macroelectronics has been display-centric, a number of applications where macroelectronics is needed to enable solutions that are otherwise not feasible are beginning to attract technical and/or commercial interest. In this paper, we discuss the application drivers and the technology needs and device performance requirements to enable high performance applications to include RF systems.*

**Keywords**—Flexible electronics, large area electronics, macroelectronics, thin-film transistors (TFTs).

## I. INTRODUCTION

Flexible, large area electronics using amorphous silicon (a-Si), low temperature polysilicon (LTPS), and organic and inorganic nanostructured semiconductor materials is a technology that is beginning to show tremendous promise. Thin-film electronics, such as thin-film transistors (TFTs) using a-Si and LTPS on rigid silicon and glass substrates are mature technologies, primarily employed for driving active matrix liquid crystal displays (AMLCDs) and image sensors but also for photovoltaics to power remote or portable electronics. A major reason for the success of these TFT-centric solutions is that solutions based on commercial silicon IC microelectronics would not be economically viable.

Microelectronics technology has revolutionized computing and communications associated with all manner of systems. As device scaling continues, and we move fully into the age of “systems on a chip” and “systems in a package,” these advances will not only continue, but become more pervasive. Yet, as revolutionary as microelectronics has been, there are functions that are not well addressed by conventional microelectronics technology. Since the driving force behind microelectronics has been smaller and smaller

devices in smaller and smaller areas, those applications that require the electronics to be spread over a large area (macroelectronics) are difficult or cost-prohibitive to achieve with the conventional approach. An example of this shortcoming can be understood by consideration of an active matrix flat panel display. Here, there is a requirement for electronics control at each pixel of the display that might cover an area as large as 1 m<sup>2</sup>. Other examples include solar cell arrays where photo diodes must be spread over areas as large as several square meters to collect sunlight sufficient to run the equipment of interest, and x-ray imagers large enough to capture images of the body without the requirement for photographic film. In a similar fashion it is desirable to have the capability of spreading electronics over a surface in order to control or modify the surface characteristics or to monitor the conditions over a large surface and not just at a specific local site.

Establishing a viable manufacturing technology for macroelectronics not only could result in lower cost electronics for certain applications, but the ability to fabricate devices over large areas on flexible substrates would provide a distributed, yet integrated, electronics capability for large area applications. Further, with a flexible substrate, the electronics package might be folded or rolled up for storage when not operational. By reducing cost and complexity of electronics and using a flexible substrate, it becomes easier to distribute the overall electronics package over an entire structure or area. To achieve these objectives a number of technical challenges must be overcome. If existing IC methods are to be replaced (augmented) in important electronics applications, then the materials, processes, and devices available with current macroelectronics technology must be significantly improved.

While electronic components like packaged ICs, resistors, capacitors, inductors and various other passive elements such as printed antennas on flexible substrates (RF on flex) have been in use in one form or another for more than a decade, what has not been achieved is the incorporation of active circuit elements such as diode and transistor arrays onto flexible substrates. Such integration could have many advantages in achieving space and weight reduction compared to standard printed circuit board (PCB) approaches. While valuable, the chip-on-flex method is limited when the active (transistor-based) electronics must be distributed over a large area (such as displays and imagers mentioned above). The advantages of large area active electronics and the multiple possible form factors and weight/space savings of flex has created a driving force to combine these two capabilities. While the initial interest is in replacement of existing products, there are many opportunities for new applications and capabilities. To differentiate this concept from well-known, existing technologies and because both the transistor dimensions (compared to ubiquitous “microelectronics”) and the product applications tend to be large sized, we refer to this class of technology as “*Macroelectronics*.”

The solution to the flat panel display, solar cell array, and x-ray imager problem is based on TFT-on-glass technology. As noted above, methods have been developed to deposit and process material that provides a large area, integrated device array that delivers the required electronic function. Extension

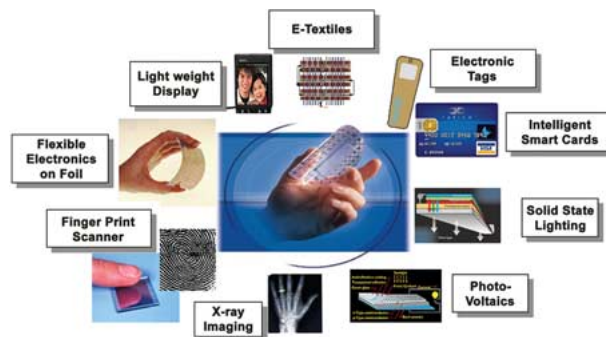


Fig. 1. Flexible TFT arrays enabling technologies for a whole range of applications.

of these approaches to flexible substrates has many potential advantages. This “next generation” flexible electronics can be viewed as the creation of large area, monolithic ICs, much as the creation of solid state ICs replaced interconnection of discrete parts on a circuit board. However, here the substrate is a flexible support structure, rather than a silicon wafer. The dimensions of the transistors need not be sub-micrometer as is the case for today’s chip-based microelectronics. Rather, micrometer-sized (1–10 μm) features are acceptable and will facilitate cost-effective manufacture. While such device dimensions will not provide the highest possible performance, there are applications for electronic solutions where high performance is not required. Rather, the driving requirements are sensing/control of a large surface area, reduced system weight/volume/cost, or flexible form factor to allow integration of the electronics package into the physical structure. For example, if a conformal distributed electronics platform were available, a number of distributed sensors, antenna, and lighting elements could be integrated to provide true real-time sensing and imaging of objects. These could be used in military and avionic applications. Conformal electronics with integrated high-sensitivity imaging and sensing elements would enable three-dimensional (3-D) medical imagers. Another interesting application with potential to become pervasive is wearable electronics.

To help reach this goal, a variety of technologies to fabricate distributed electronics based on TFTs and flexible substrates are under investigation. The ultimate purpose is to create a technology infrastructure that enables electronic solutions not feasible with today’s existing microelectronics-based manufacturing methods. If successful, macroelectronics will open up a large set of applications that are not currently served by Si CMOS adequately, as shown in Fig. 1. The rapid commercialization and adoption of macroelectronics ultimately depends on cost and performance metrics for the given application.

While there are a number of new research initiatives on large area macroelectronics around the world, in the following section, we would like to discuss important aspects of the Macroelectronics program funded by the Defense Advanced Research Projects Agency (DARPA), which is exploring the technology as a solution for a variety of problems. Over the last ten years, there were a number of DARPA-sponsored research initiatives in flexible displays, direct write electronics, thin-film photovoltaics, and batteries

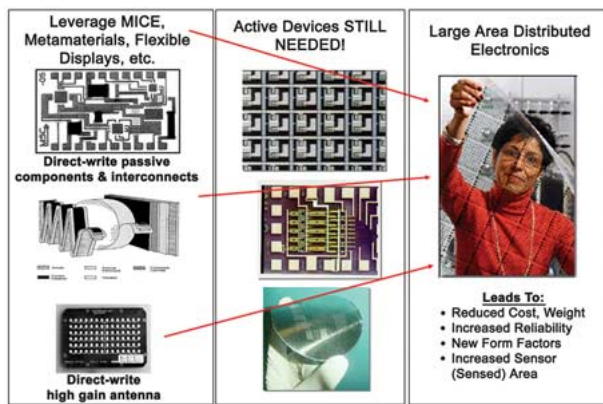


Fig. 2. Overview and objectives of the Macroelectronics program.

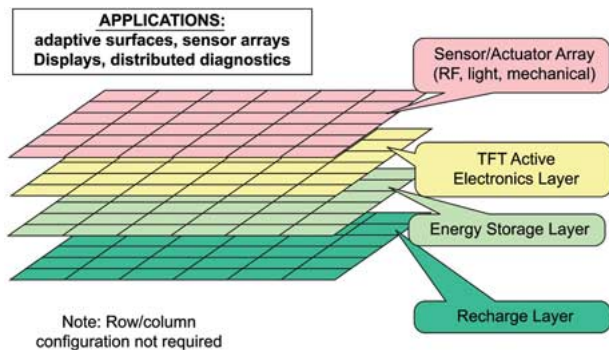


Fig. 3. Functional building blocks for a generic macrosystem.

that created the foundation to build macroelectronic systems (see Fig. 2).

What the *Macroelectronics* program aims to achieve with these diverse technologies is to help develop the necessary application infrastructure to build high-performance systems. The current programs go beyond the limitations of the current-generation TFT technology to adopt and develop relevant manufacturing methods to provide integrated processing. In the case of improving TFT performance, this program proposes a paradigm shift by using nanomaterials and novel inorganics to allow electronic feature sizes to become bigger while maintaining acceptable performance. Ultimately, all the building blocks necessary to build a macroelectronic system as suggested by Fig. 3 should be possible.

## II. APPLICATION DRIVERS

Many of the most demanding military and aerospace electronics applications are space-, weight-, and power-(SWAP) constrained, yet the components must be kept affordable if the overall system is to be viable. Advanced technologies that address both the SWAP and cost factors of future electronics are critical to maintaining the dominant position in military systems. Therefore, the goal of the *Macroelectronics* program is to develop novel form factor technologies with the potential for increasing the utility of electronic subsystems while at the same time offering significant cost reductions over the existing paradigm. To reach this goal, the emphasis of the *Macroelectronics* program is

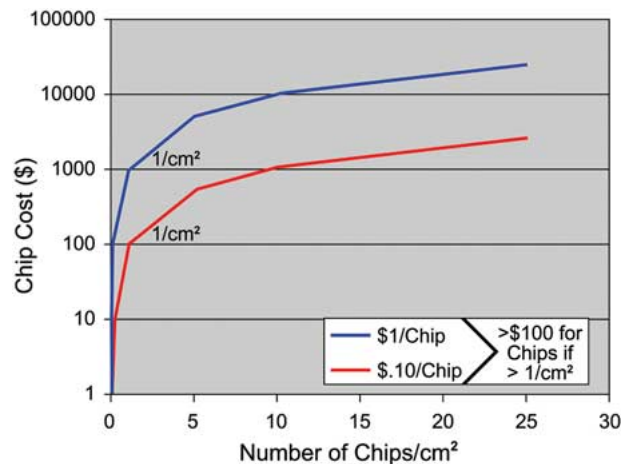


Fig. 4. Cost assessment for macroelectronic application shows that packaging large numbers of Si ICs becomes very expensive when the surface area exceeds 1000 cm<sup>2</sup>.

to identify and develop innovative technology to fabricate distributed electronics based on TFTs and flexible substrates. Specifically, the performance of TFTs will be comparable to that associated with bulk semiconductor devices of similar dimensions while cost-effectively manufactured on flexible substrates. Development of this capability will be closely coupled with system designers to ensure that proposed *Macroelectronics* solutions meet all the technical and cost requirements for a variety of large area, distributed, flexible electronic subsystem applications. The ultimate purpose is to create a technology that enables electronic solutions not feasible with today's existing microelectronics-based methods. Examples include such diverse functions as diagnostic, control, and sense functions to manipulate the properties and environment over a large surface (not just at discrete points), integration of the electronics into the structure in order to free space/weight for other system functions such as fuel, sensors, etc., or better human I/O interface in electronic systems.

Additionally, while many other significant technology advances must occur, *Macroelectronics* may also provide technology to facilitate advanced prosthetics such as described in previous work on "sensitive skins" [1].

Silicon CMOS wafers typically cost about \$10/cm<sup>2</sup>, and compound semiconductors are even more expensive. Thus, if many chips are required per subsystem the cost of just the components can become prohibitive. A simple cost analysis highlights the issue at hand. For example, a cost assessment for microelectronics and macroelectronics for large area applications shown in Fig. 4, summarizes the cost differential between the solutions for a distributed electronic application with a 1000-cm<sup>2</sup> area. A discrete IC solution is >\$100 for just the components. Assembly costs can further increase cost significantly. In contrast, the goal of the *Macroelectronics* program is \$0.1/cm<sup>2</sup> (\$100/1000 cm<sup>2</sup>).

Of course, low cost is no advantage if operation cannot be achieved for relevant classes of problems. Hence, performance must be significantly enhanced for solutions to be viable. While cost is a significant factor in the drive to create

a Macroelectronics technology, enhanced reliability matters too. Rather than individual wires connecting a large number of components on a surface, macroelectronics will enable the simultaneous integration of all components onto the substrate. From this perspective, the advantage is analogous to the conversion from hybrid circuit technology to IC technology: the key difference, of course, being that macroelectronics will produce a really, really big chip.

One of the most important and most challenging applications for the proposed macroelectronics technology is extending current TFT technologies to reach the RF levels of performance needed to support very large, lightweight, low-cost, active, electronically scanned antennas for Department of Defense (DoD) communication and surveillance systems. A multidisciplinary team is developing higher performance TFT fabrication and materials technologies, enhanced TFT design tools and software, and low-cost manufacturing techniques for large area RF circuits on flexible plastic substrates. The goal is RF circuit performance at over 500 MHz with applicability to large military active antenna systems operating in the UHF or higher regime.

Given today's geopolitical climate, the pressure to improve the mission capability of unmanned aerial vehicles (UAVs) is very high. The space, weight, power, and cost of UAV avionics is driving engineers to look for alternative methods of incorporating antennas and their associated electronics into UAVs. However, current state-of-the-art airframe designs have been pushed to their limits. Communications and additional electronic capabilities are desired without compromising vehicle performance.

Many next-generation military RF surveillance systems require very large active antenna arrays which are flexible and conformal. Targeted systems include UAVs with antennas conformally mounted to wing surfaces, airships with large conformal antennas, and space systems which must have antennas stowable in a small volume for liftoff and then deployable in orbit to cover a large area. Antenna sizes of up to 5000 ft<sup>2</sup> or more are needed for these systems. Extremely low weight is critical for airborne or space-borne applications, and low cost is required to attain system affordability goals. Flexible plastic antennas incorporating flexible active circuitry are ideal candidates to meet these requirements. Active circuitry on these antennas includes low noise amplifiers (LNAs), RF switches, active RF combiners, and digital control circuits. A number of these systems operate in the UHF frequency range (~500 MHz), while others operate at S-band (5 GHz) or X-band (8–12 GHz). The UHF systems have antenna diameters of up to 150 ft. While Si-based TFTs may be able to support UHF applications, higher performance devices will be needed to address S- and X-band operation.

State-of-the-art antennas used to perform the above functions are built today as stand-alone units. These antennas are secondarily attached to the aircraft as fairings or protruding surface mounted systems and are hard-wired to signal processing and control systems within the platform. Protruding antennas have a number of drawbacks including reduced aircraft endurance due to increased drag and weight, and in-

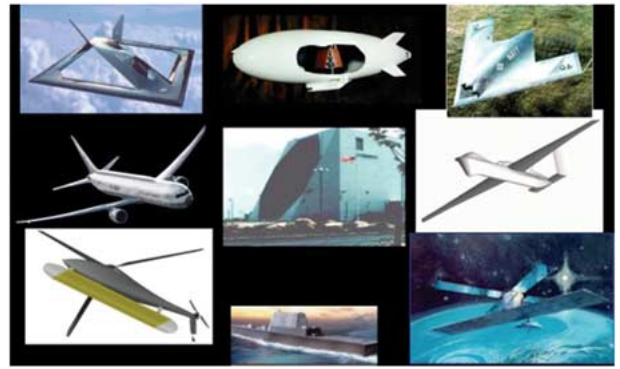


Fig. 5. Military applications requiring large active antennas.

creased RF signature and required maintenance due to their protruding nature. In addition, the electronics and associated signal conditioning modules used to amplify, control and process the signals from conventional antennas account for a significant portion of the weight and space of the avionics system. Hence, there is a need for conformal, nonprotruding antenna systems with integrated electronics that overcome the deficiencies of conventional systems. Conformal arrays with integrated electronics, such as a transmit/receive (T/R) module, offer significant benefits to the platform, including the following.

- Increased aircraft endurance and integrity due to reduced drag and weight (by eliminating protruding antennas and parasitic support structures, and reducing the amount of wiring and associated cut-outs in the structure).
- Increased performance due to larger apertures, reduced losses by integrating the electronics in closer proximity to the radiating elements, and greater flexibility in selecting antenna placement locations on the platform.
- Multi- and/or wide-band RF performance and graceful system degradation due to increased control with integrated electronics.
- Reduced cost and downtime associated with maintenance due to reduced overall system complexity.
- Reduced RF signature of the platform (by eliminating protruding structures).

One of the demonstration vehicles for the program will be a multichannel antenna subarray fabricated and tested in the final phases of the project. The subarray will include low noise amplifiers, RF switches, combiners, and power regulation using macroelectronics TFT-based active components, and matching networks and delay lines using macroelectronic passive components implemented on the large flexible substrate. The final demonstration will consist of a 2 ft × 2 ft flexible UHF radar antenna segment containing UHF-capable flexible TFTs, which can demonstrate scalability to the larger sizes needed by emerging systems. Ultimate military platforms for the technology include unmanned airborne surveillance craft, airships, and ship-borne/space-borne arrays, illustrated in Fig. 5.

Another goal of the large area electronics effort is to explore textile materials and textile manufacturing for building

VHF, UHF, and microwave antennas. The technology would then be exploited to manufacture novel electronic products. Examples are being applied at frequencies from VHF through microwave in both active and passive applications. The result is an ability to produce very large, lightweight, low-cost and, if desired, flexible antennas for a variety of terrestrial, airborne, and space-based applications.

Textile techniques utilize computer-controlled volume-production manufacturing techniques to build sophisticated arrays with the tolerances and repeatability afforded by computer-automated textile processes. The result is lighter weight and lower cost antennas than existing solutions. Electronic textile manufacturing methods (such as computer-automated embroidery of conductive threads, laser-cutting and adhesion of conductive cloths, nonwoven techniques, and metallic knits for building custom antennas) are being investigated. The resulting antennas can also be encapsulated into composite structures that could include textile substrates to provide man-portable antennas for enhanced communications and identification of friendly forces.

While RF is a dominant and daunting challenge for applications of TFT to large area electronics, there are other opportunities with significant operational payoff. The ability to efficiently utilize the surface areas of large structures as part of an intelligent sensor network will allow a larger, highly responsive, complex system for real-time monitoring and response. Electronics embedded with sensors over a surface would provide area (versus point) coverage and provide local processing of the sensor data to include amplification, signal conditioning, routing, and switching. Maintenance of a real-time operational database of structural information can permit early warning of degradation, damage and the potential for catastrophic failure, thereby minimizing a structure's lifetime cost.

The performance and behavior characteristics of nearly all in-service structures can be affected by degradation resulting from sustained use as well as from exposure to severe environmental conditions or damage resulting from external conditions such as impact, loading abrasion, operator abuse, or neglect. These factors can have serious consequences on the structures as related to safety, cost, and operational capability. Therefore, the timely and accurate detection, characterization, and monitoring of structural cracking, corrosion, delamination, material degradation, and other types of damage are a major concern in the operational environment.

Structural health monitoring (SHM) is increasingly being evaluated by the industry as a possible method to improve the safety and reliability of structures and thereby reduce their operational cost. SHM technology is perceived as a revolutionary method of determining the integrity of structures involving the use of multidisciplinary fields including sensors, materials, signal processing, system integration, and signal interpretation. The core of the technology is the development of self-sufficient systems for the continuous monitoring, inspection, and damage detection of structures with minimal labor involvement. The aim of the technology is not simply

to detect structural failure, but also provide an early indication of physical damage. The early warning provided by an SHM system can then be used to define remedial strategies before the structural damage leads to failure.

Another capability the program is developing is novel SHM technologies through the use of built-in distributed sensor networks integrated with composite and metal structures. The basic idea of the technology is to use a network of distributed piezoelectric sensors/actuators embedded on a thin dielectric carrier film to monitor and evaluate the integrity of a structure. A diagnostic unit is used to collect and process signals obtained during the monitoring process. The signals can then be analyzed to determine the integrity of the structure. In active mode, actuators generate preselected diagnostic signals and transmit them to neighboring sensors whose response can then be interpreted in terms of damage location and size or material property changes within the structure. In passive mode, the system can be used as a continuously monitoring sensor network. Both modes permit real-time structural analysis and evaluation along with constant collection of structural data and information while the structure/vehicle is in service. Current systems are being tested for use in a variety of applications such as in the monitoring of crack growth, bond-line repairs on multi-riveted metallic joints and composites, hot spot monitoring of inaccessible parts such as landing gears, monitoring of machined parts such as frames and fittings, and monitoring of pressure vessels. The technology can be employed to constantly monitor critical areas on in-service structures, equipment, and vehicles.

A major drawback of the existing technology is in its networking capability with a multitude of sensors applied to physically large structures. The greater the number of sensors, the greater the number of wires and electronics required to connect and work with them. Although increasing the number of sensors can to some extent improve the resolution of detection of damage in a structure, it can at the same time increase signal noise. Therefore, scalability of the technology can be a major challenge. This issue can slow down the time required to inspect a structure using a SHM system and increase the cost of inspection. Both factors can limit the use of the technology.

In order to resolve these issues, it is vital to reduce the number of controlling wires and sensors on a structure. One possible method to do this would be to use built-in switches using TFT technology. The goal of the effort is to develop a SHM system that can be applied to structures of any geometry and configuration and has the capability for enhanced damage detection using embedded control of the actuators and sensors. The system will be versatile for application to large or small (hot spot) structures that utilize a large number of sensors and will be low cost.

Since nearly all in-service airborne, ground, and sea-based vehicles, buildings, space, and weapons system platforms require some form of inspection and maintenance procedures to monitor their integrity and health condition, to prolong life span, or to prevent catastrophic failures, the potential applications of the developed system are very broad. Some near-

term applications include large-scale rocket motors, military and commercial aircraft, and reusable space launch vehicles.

The interest in higher performance, large area electronics is not limited to the DoD. NASA is developing a variety of deployable space system concepts for future missions where very large structures are required. Examples are large aperture radars ( $> 400 \text{ m}^2$ ), optical telescopes ( $> 10\text{-m}$  diameter) and solar sails (meter to kilometer wide). For these missions, low mass and volume systems such as thin-film membranes with new lightweight deployment systems such as inflatable and rigidizable structures are required. These membrane systems will require integrated sensors for health monitoring and shape sensing and in some cases shape control. To keep the mass low (e.g., mass density of  $2\text{--}4 \text{ kg/m}^2$  for large aperture radars and a few grams per meter squared for solar sails), it is essential to integrate the sensors with the membrane. Therefore, macroelectronics is expected to be a critical enabling technology if these demanding missions are to be achieved.

Recent measurements of solid-earth surface deformation using interferometric synthetic aperture radar (InSAR) have enabled major advances in the scientific understanding of crustal deformation associated with seismicity. InSAR techniques are capable of providing centimeter-level surface displacement measurements at fine resolutions (tens of meters) over wide areas (hundreds of kilometers). Next-generation, large aperture ( $> 400 \text{ m}^2$ ) InSAR systems hold the promise of providing data that could better the scientific understanding of global earthquake physics to the extent that they might ultimately lead to an earthquake forecasting capability [2], [3]. These SAR systems will provide fine temporal sampling (on the order of hours to days) in order to capture the subtle effects associated with fault interactions and strain accumulation between earthquakes. Moreover, revisit times on the order of minutes can be used for disaster response scenarios.

The extremely large mass and stow volume of the current rigid manifold phased array antennas will make it almost impossible for the radar to fit in existing launch vehicles [5], [6]. Therefore, for such large apertures, new technologies such as the Jet Propulsion Laboratory's (JPL's) lightweight membrane antenna shown in Fig. 6 are ideal. Where membrane-based antennas are assumed, conventional packaging technologies are currently being considered for placement of T/R modules [7]. Although innovative, this approach has reliability challenges in addition to the high cost of integrating individual electronic components. Hence, the macroelectronics approach is a paradigm shift that could solve these issues.

Two critical problems need to be solved before active membrane antennas can be implemented in space.

- 1) Array calibration: Since a membrane-based antenna lacks structural rigidity, the array is prone to deformation due to thermal and mechanical forces. In turn, this affects the phase stability of the array and compromises its performance. Therefore, macroelectronics-based sensors for detection and correction

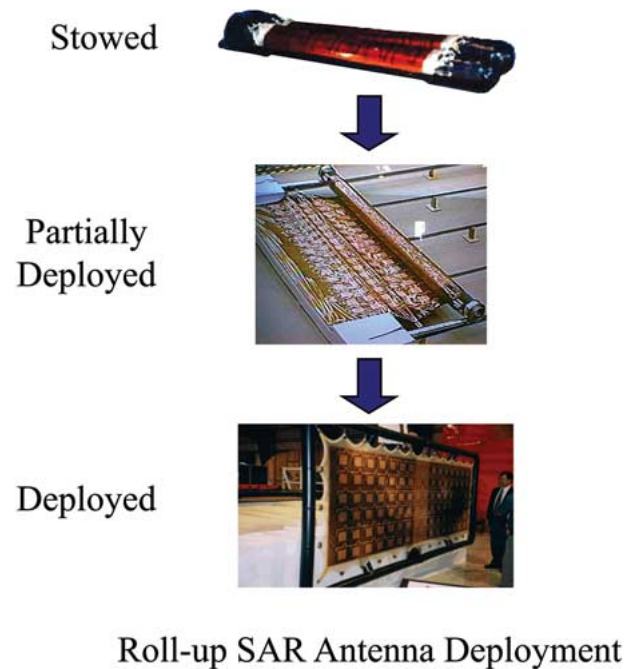


Fig. 6. Passive membrane antenna for SAR applications [4].

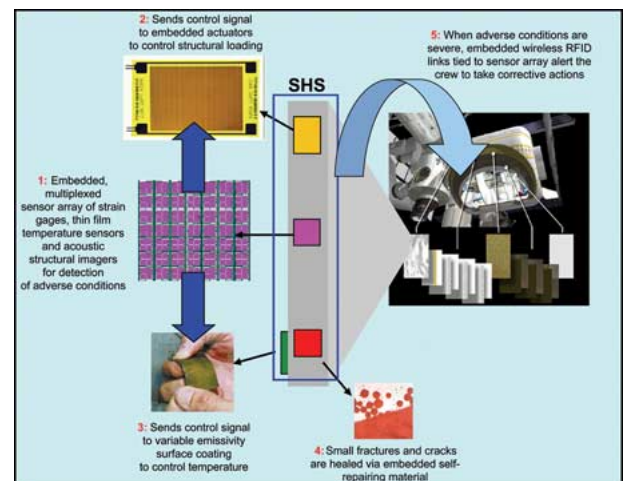


Fig. 7. A conceptual view for a proposed structural health system, based on integrated sensing and adaptive capabilities (Courtesy of Erik Brandon at JPL). The development for this system is currently supported by the NASA Exploration Systems Research and Technology (ESR&T) Program.

of parameters such as planarity and temperature are essential. Other health monitoring components, such as sensors for detecting tears and punctures, are also required.

- 2) Integration of T/R modules with the membrane: Due to the number of T/R modules on a very large array, macroelectronics-based T/R modules can assist with integration, reliability, performance, manufacturability, and cost of active membrane antennas.

Additional applications for macroelectronics-based solutions are also anticipated. Fig. 7 shows a conceptual health monitoring system for the TransHab space habitat [8]. A real-time health monitoring system for detecting adverse

conditions and their location and initiating corrective actions is critical to improving crew safety and the time spent monitoring structural problems and their repair. This system is composed of a network of integrated thin-film sensors and control mechanisms embedded into the multilayer structure. Structural defects and cracks will be detected and located automatically; for smaller defects, a passive self-healing mechanism will correct the problem. Embedded actuators interfaced with embedded strain gages will be used for controlling static and dynamic loads. Integrated temperature sensors and variable emissivity material will be used for temperature control of the habitat. Integrated TFT technology will enable these low mass future systems.

Another example of the potential for large area electronics is for remote sensing of deep space and the cosmos. This relies on increasingly larger and larger telescopes with increased sensitivity and spatial resolution. The James Webb Space Telescope, a 6-m telescope flying at L2, will identify and study the first stars born in our universe. SAFIR, a 10-m mid- and far-IR telescope, will probe the formation of planetary systems in our galaxy. The Terrestrial Planet Finder, an 8 m × 4 m telescope, will image Earth-like planets around nearby stars and give us crude spectra of their disk-integrated atmospheres and surfaces. Succeeding generations of space telescopes will be larger and require even greater optical precision, which is only achievable by driving down the mass of a telescope's collecting area while increasing our ability to achieve and maintain the precise optical figure needed to obtain pristine images.

Integrated macroelectronics would represent an enabling technology for these future telescopes. Fine-grained active thermal control for both telescope mirrors and support structures using integrated sensors, heaters, and variable-emissivity elements will minimize thermal deformations and the resulting aberrations, leading to low-mass telescope designs which in turn would allow large collecting areas to be launched. Active shape control of optical surfaces using embedded/integrated shape sensing and actuator elements will lead to further improvements in the key kilograms per meter squared area density metric. Along this technology path are large (>10-m-diameter) membrane mirrors, with layers of reflective material, structural support, and macroelectronic sensing and control elements which maintain precise figure control. With these large lightweight mirrors, the telescopes of 2020 and the years beyond will cost-effectively tackle future scientific challenges.

### III. HIGH-PERFORMANCE DEVICES

While current TFT technology is highly developed, it is limited in what applications it can address. For instance, a major interest is to apply TFT technology to flexible substrates. Significant effort has been made to provide this capability for displays, but with only limited success. Further, TFT circuit performance has been limited by relatively poor device characteristics compared to bulk Si. Existing methods are constrained by materials and/or substrate process limitations and result in TFTs with low mobility that supports only

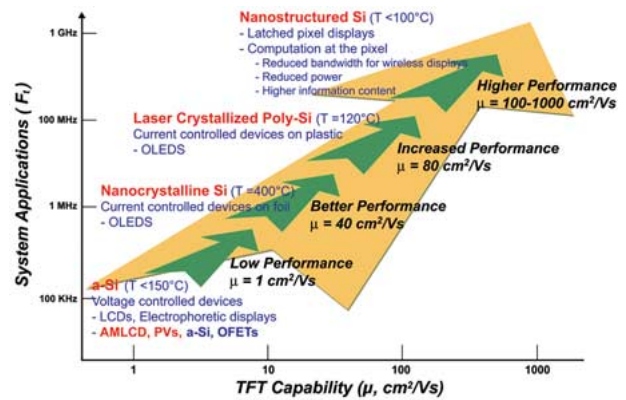


Fig. 8. Capabilities of the TFT backplanes versus system applications which can be enabled.

low-frequency circuit operation. Thus, applications that require even modest computation, control, or communication functions cannot be addressed by today's TFT technology. To achieve the desired ability to implement large area electronic functions, it is necessary to significantly improve TFT device performance and to develop cost-effective fabrication methods that are compatible with flexible substrates.

Flexible circuits built with existing a-Si and LTPS device technologies have mobilities one to two orders smaller than those built on crystalline silicon. To highlight the need for higher mobilities, we present in Fig. 8 a map of mobility versus applications that can be enabled for a particular mobility regime.

While device structures and materials with high electron mobility to achieve high performance are the focal point of the effort, there are several other factors that must also be considered. Perhaps most significant is the need for thin, but reliable, gate dielectrics to allow relatively low voltage operation. Low-resistance ohmic contacts will also be essential to minimize the effects of parasitics on device performance. Since it is difficult to make small devices over large areas, it is essential to minimize parasitics which degrade RF performance from that based on semiconductor material parameters. From a circuit perspective, high device yield and uniformity must be achieved. Finally, the metal interconnects must provide both low resistance and durable, rugged performance when the substrate is flexed.

Because there is significant literature already available that describes efforts at improving the device/circuit characteristics of conventional Si-based TFTs, no description of their current status is needed here. The interested reader is referred to the review papers in the current issue of this journal, recent publications [9], and several excellent reference volumes [10], [11]. Instead, efforts that focus on device design and novel device concepts seeking to overcome current limitations and extend TFT technology into new macroelectronic arenas are summarized.

Current TFT fabrication and design techniques have not been optimized or even evaluated for application in the military frequency ranges of interest described above. Performance for RF applications is being addressed by developing high-mobility polysilicon TFTs using temperature-annealed

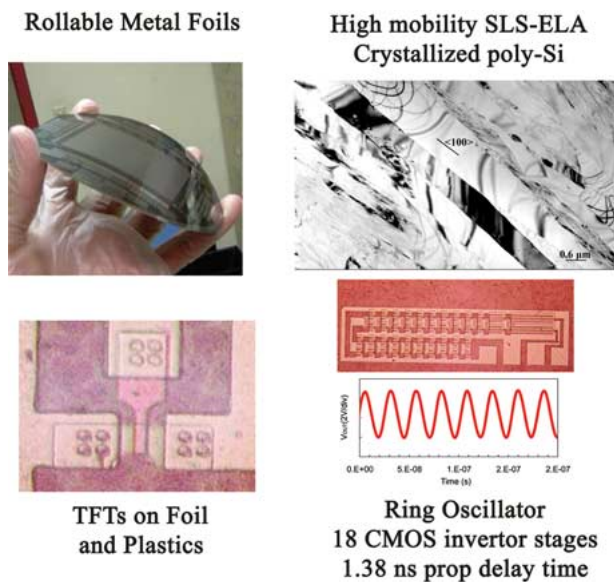


Fig. 9. TFTs are currently being fabricated on flexible metal foils with performance of several hundred megahertz.

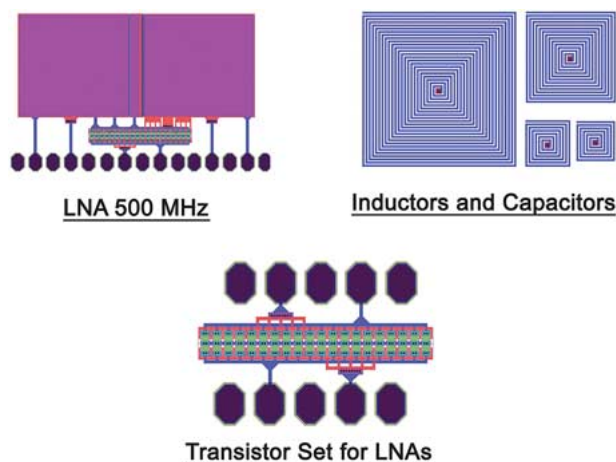


Fig. 10. Next-generation TFT fabrication runs on metal foils and plastic films consist of RF designs and other features supporting accurate model parameter extraction.

and laser-crystallized techniques. RF TFTs also need relatively short ( $\sim 1 \mu\text{m}$ ) and wide ( $400 \mu\text{m}$  or more) transistor sizes. Issues of scalability, low gate resistance, and low on-resistance are being addressed for low-noise amplifiers (LNAs) with high gain and low noise figures and low-loss switches. These improved TFTs are currently being fabricated on thin flexible metal films, with a digital circuit performance of several hundred megahertz, as shown in Fig. 9 [12]–[15].

A next generation of designs is now underway containing a number of RF structures, as shown in Fig. 10. Techniques for fabricating these TFTs directly on flexible plastic films with higher performance and lower cost are also underway.

The Macroelectronics project is also exploiting advanced modeling capabilities by enhancing AIM-SPICE to provide capability for modeling RF circuits. Extending the modeling capabilities down to  $1\text{-}\mu\text{m}$  channel lengths has been performed, and noise modeling and S-parameter capabilities are

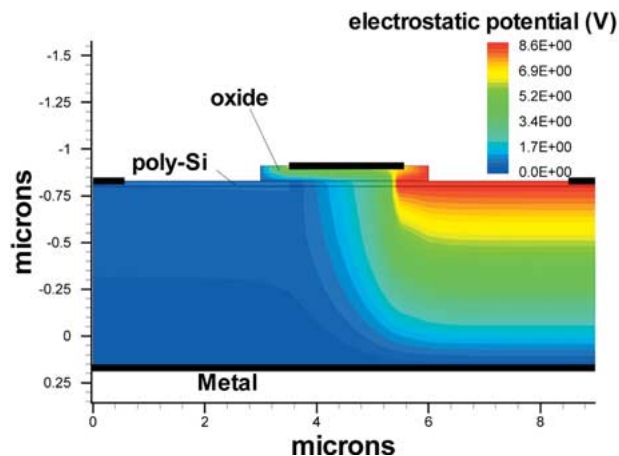


Fig. 11. TFT modeling enhancements include 2-D visualization.

being incorporated. The modeling is also being fitted with extracted data from the high-performance TFT process, providing RF designers capabilities for designing radar circuits. Two-dimensional (2-D) models, shown in Fig. 11, are also in development to provide a higher level of model fidelity and assistance in improving TFT reliability.

In order to enhance the performance of TFTs, laser crystallization has been the industry approach. Among the various crystallization approaches, sequential laterally solidified (SLS) silicon is a preferred method to achieve high mobilities. In SLS, laser crystallization of an a-Si film is performed using a patterned excimer laser beam sequentially flashed onto the film, leading to large-grain polycrystalline silicon, or even single-crystal silicon regions [16], [17]. This method is distinct from the excimer-laser annealing method, which in general provides lower TFT mobilities and has lower equipment throughput. SLS crystallization to produce high-mobility TFTs for displays on glass substrates is in production [18]. But SLS has only very recently been implemented on polymer substrates as part of the DARPA Macroelectronics Program, with n-channel field-effect mobilities greater than  $400 \text{ cm}^2/\text{V} \cdot \text{s}$  on polymer substrates recently achieved [19], [20]. Successful development of SLS crystallization on flexible substrates will be a major enabler for a variety of new applications.

For even higher performance applications, compound semiconductors are the material of choice just as with conventional crystalline microelectronics. Therefore, given the potential of SLS to provide quality polycrystalline Si, it is also of interest to explore SLS for other semiconductor materials. Such materials as Ge, GaN, SiC, and InP can in principle be deposited at low temperature and heated via laser to crystallize areas large enough and with mobilities high enough to provide useful device characteristics. Among the additional challenges in successfully developing this approach is the requirement to deposit and anneal in the appropriate background ambient to achieve the appropriate elemental ratios for the crystallized materials.

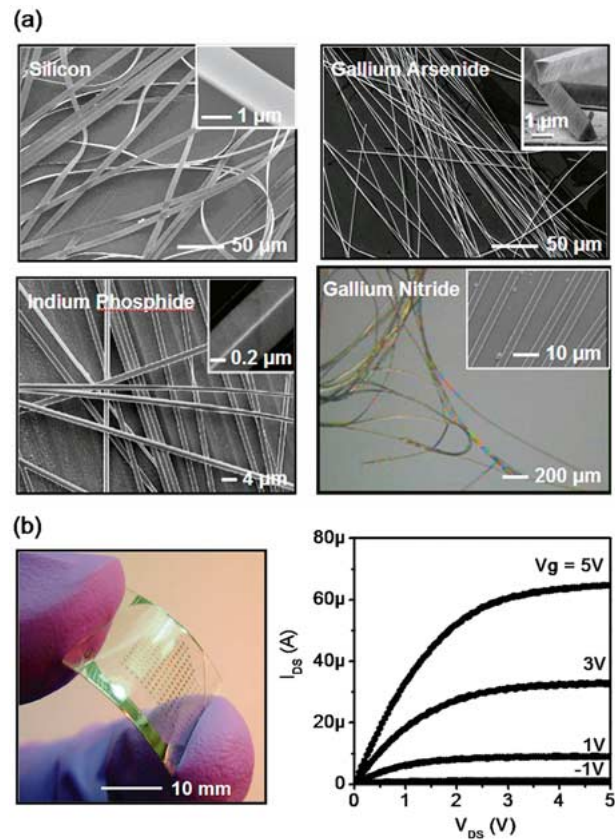
Recent results promise far better TFT devices from certain polycrystalline compound semiconductors than from polysilicon. Polycrystallinity means a high concentration of grain

boundaries, which normally degrade the transport properties [21] of polycrystalline transistors by means of Fermi level pinning. Even more strongly than silicon, most (but not all) III–V compound semiconductors, pin the Fermi level midgap at surfaces such as grain boundaries, resulting in large barriers to transport, depletion of the grains' interiors [22], and lowering the conductivity. Fermi level pinning at the interface to the gate also prevents field-effect modulation of a channel's conductivity, further degrading transistor performance [23].

Poly-InAs, however, remarkably exhibits two anomalous properties. First, its surface Fermi level pins *above* the conduction band edge, resulting in accumulation rather than depletion at surfaces such as grain boundaries [24], [25]. Second, its electron effective mass is about an order of magnitude lighter than silicon's, resulting in proportionately higher mobility. These two properties in combination greatly reduce the barrier to carrier transit across grain boundaries and throughout highly defected material. Furthermore, the wide separation between the conduction band minimum and satellite conduction band valleys is predicted to support a peak saturated drift velocity of about  $8 \times 10^7$  cm/s in single-crystal material [26], which is at least an order of magnitude faster than the  $v_{\text{sat}}$  of ideal single-crystal silicon. Thin films of InAs have been under development since 1968, and have already demonstrated electron mobilities [27], [28] in the range of  $800\text{--}3000$   $\text{cm}^2/\text{V} \cdot \text{s}$ . These experimental results are consistent with InAs TFTs achieving cutoff frequencies above 1 GHz for a  $10\text{-}\mu\text{m}$  feature size and above 10 GHz for  $1 \mu\text{m}$   $L_g$ . If these results can be integrated into large area processing and extended perhaps to other semiconductors, a major limitation of TFT-based electronics could be circumvented.

As deposition and crystallization of semiconductors on flexible, low-temperature substrates is a significant problem, nonthermal means of providing high mobility semiconductors are also being explored. These approaches include TFTs made from microstructured silicon or nanowire transistors. Both have the capability to provide highly crystalline semiconductor materials by a variety of printing/deposition methods that do not require thermal processes to achieve high-quality semiconductors. This approach uses micro/nanoscale objects—nanotubes, nanowires, ribbons, disks, platelets, etc.—of high-quality single-crystal semiconductors. A collection of these building blocks constitutes a type of material that can be deposited and patterned, by dry transfer printing or solution casting, onto plastic substrates that forms an effective semiconductor layer to yield mechanically flexible TFTs that have excellent electrical properties [29]–[34]. Because this approach separates the semiconductor growth process from the device substrate, it is independent of traditional requirements for epitaxy, thermal budgets for processing and other considerations. As a result, it is well matched not only to flexible electronic systems on plastic substrates but also to devices that require heterogeneous or 3-D integration.

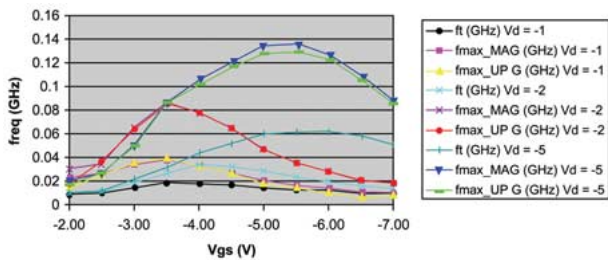
A key feature of these objects is that they are formed directly from conventional wafers using lithography and



**Fig. 12.** (a) Optical and scanning electron micrographs of wires and ribbons of single-crystal inorganic semiconductors, produced by lithographic processing of conventional wafers. Collections of these elements can be printed onto low-temperature substrates, such as plastics, to form the semiconductor component of flexible electronic devices. (b) Image (left) of an array of TFTs on plastic which use printed silicon ribbons as the semiconductor, and typical current–voltage characteristics (right) from one of these devices. The performance of devices of this type can approach that observed in conventional silicon MOSFETs [31], [32].

etching steps. As a result, they naturally exploit the highly developed crystal growth and doping technologies that have emerged from decades of effort in the semiconductor industry. Solution or dry transfer printing them onto plastic substrates can yield high-performance flexible TFTs. This type of approach has been successfully demonstrated for highly bendable device arrays of modest size [left frame, Fig. 12(b)], and it is scalable to large areas [30], [32]. The right frame of Fig. 12(b) shows the characteristics of a typical device that uses an organized array of silicon ribbons. The level of performance—mobilities greater than  $300 \text{ cm}^2/\text{V} \cdot \text{s}$ , on/off ratios as high as  $10^6$  exceeds, by a large margin, the previous best for transistors formed by printing onto plastic substrates.

Although the problems associated with thermal deposition and recrystallization are circumvented with this approach, for low-temperature processing the challenge of achieving high gate dielectric integrity remains, and there is the additional difficulty of achieving low-resistance source and drain contacts without performing a high-temperature implant activation step, which may require laser processing of the source–drain regions. One strategy to avoid these

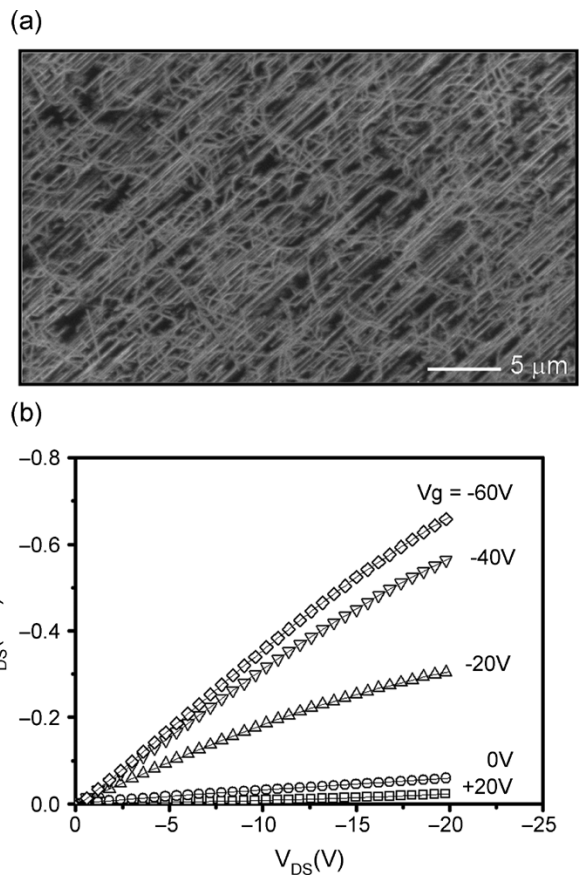


**Fig. 13.**  $f_T$  and  $f_{\max}$  calculated from S-parameters taken at multiple bias points.  $V_d$  was set at  $-1$ ,  $-2$ , or  $-5$  V and  $V_g$  was swept from  $-2$  to  $-7$  V.  $f_{\max}$  was calculated from both maximum available gain and from unilateral power gain.

problems involves growing the dielectric and performing the doping before the semiconductor is printed onto the low temperature substrate [33]. Even without these types of schemes, however, work to date indicates that mobilities of  $> 200 \text{ cm}^2/\text{V} \cdot \text{s}$  can be achieved for devices with channel lengths sufficiently long that the effects of the Schottky contacts do not severely degrade device performance. Non-RF optimized devices fabricated with the nanoribbon/wire approach with gate lengths of  $2 \mu\text{m}$  have shown  $f_T$  of over 100 MHz (see Fig. 13). Even better results can be expected for compound semiconductor devices which can also be fabricated via this method.

Single-wall carbon nanotube (SWNT) TFTs have received significant attention for microelectronic applications recently because of their unique properties, including potential mobilities of  $10\,000 \text{ cm}^2/\text{V} \cdot \text{s}$  or higher, as well as the ease and low expense of producing them in large quantities. These same properties make them attractive for large area electronics because of the potential for achieving extremely high field-effect mobilities on plastic substrates, with the semiconductor deposited from a liquid at room temperature, perhaps using printing methods [34]. For these applications, the SWNTs can exist in the form of random network [35], [36] or aligned arrays [37] between the source and drain electrodes of the TFT. Fig. 14 shows an image of an array of tubes formed by guided growth, and the output characteristics of a device fabricated with a similar collection of tubes [38]. In both the array and the network geometries, good performance can be obtained—mobilities of  $\sim 100 \text{ cm}^2/\text{V} \cdot \text{s}$  or better and on/off ratios greater than 1000. Due to the extremely high intrinsic per-tube mobilities, it is expected that very high device mobilities will be possible by increasing the fill factor of tubes from the current relatively low values of 1%–2%.

Several major challenges must be overcome in order to take full advantage of carbon nanotubes as an electronic material. A major barrier to very low temperature processing is the gate dielectric; it is difficult to form low-temperature deposited dielectrics with high dielectric integrity and with low hysteresis for the tube devices. Next, since carbon nanotubes (as-grown) consist of a mixture of semiconducting and metallic tubes, a means must be found either to remove the metallic tubes selectively or render them insulating; otherwise, the metallic tubes will act as shorts. Finally, for maximum device performance, it is desirable to have a high density of nanotubes aligned in parallel between source and



**Fig. 14.** (a) Scanning electron micrograph of an array of SWNTs formed by guided growth. The coverage of tubes in this case is  $\sim 1\%$ . (The apparent width of the tubes in this image is much larger than the actual width). (b) Current–voltage characteristics for a typical device. Mobilities larger than  $100 \text{ cm}^2/\text{V} \cdot \text{s}$  are possible.

drain; therefore, just as in the case of other semiconductor nanowires, a reliable means must be developed to orient and position the nanotubes. Here again, not only may this approach provide a means to high performance devices for large area electronics, but as with the nanowire type approach, “printing” of C nanotubes may also be a viable route to 3-D and heterogeneous integration.

An area beyond the scope of this paper is the development of model and simulations tools that can be used for device and circuit design as well as predictive engineering. Since these devices are not single “wires” or single crystals, but rather an ensemble of particles, the aggregate behavior as well as interfering effects must be considered. While only limited work has been completed to date, nonetheless, very encouraging results that provide good agreement with experiment have been achieved. Alam has developed an analytical SPICE-like compact model for TFTs based on nanobundle composites with wire density below the percolation limit [39]. They identified three variables—channel length to tube length, channel length to mean free path, and tube density to percolation density—as controlling the transport properties of macroelectronic TFTs. This model could be used to optimize nanobundle transistors and sensors and allow overall system design based on conventional SPICE-based simulation tools. Further, they developed a self-consistent

linear electrothermal percolation model for TFTs based on nanobundle composites appropriate for all densities and channel lengths. This model explains the channel length dependencies of conductance for the available experimental data published to date in the literature. The next step is to generalize this work to a self-consistent transistor model that can be used to design devices for macroelectronic applications and develop statistical VLSI design techniques for circuits based on flexible components (whose parameters may be changing randomly as a function of time) for macroelectronic applications.

Finally, a non-semiconductor solution is also being explored. An ideal technology for macroelectronics would be one that is ultrafast, compatible with nearly any substrate, requires only low-temperature processing, and is inexpensive. Metal–insulator electronics has the potential to fit that ideal because the active device is composed of amorphous materials and avoids the troublesome issues of grain boundaries.

The basic building block is the metal–insulator–metal (MIM) tunnel junction. Electrons tunnel from one metal layer to another through an ultrathin (2–3 nm) insulator on the order of 1 fs and provide diode current–voltage characteristics. Generally, these characteristics are “soft” because the metal–insulator junction produces only a weak nonlinearity. However, a double-insulator (MIIM) diode [40] exhibits dramatically sharper nonlinearity, resulting from a quantum well formed between the two insulators. It is hoped that this will enable practical thin-film diodes for rectification of ultrahigh frequency signals. Small, prototype metal insulator diodes have been fabricated and tested beyond 200 GHz. The challenge is now to develop a controlled process that not only provides the desired MIIM structure and characteristics, but one that can be fabricated reliably on flexible substrates over large areas.

The concept of a MIMIM tunneling transistor has existed for decades. In this transistor, outer layers of metal form the emitter and collector, and electrons tunnel through a thin base metal layer sandwiched in the middle, between two thin insulators, as shown in Fig. 15(a). The middle metal base region is thin enough that hot electrons injected from the emitter junction flow through the base without significant scattering. In this way, current injected into the base controls current from emitter to collector, thereby providing current gain. As with the single-insulator MIM diode, the MIMIM tunneling transistor has poor performance characteristics. A major reason for the poor performance is that the tunneling electrons have a broad energy distribution, as depicted in the figure. With a double insulator situated between the emitter and the base, the performance of the MIIMIM tunneling transistor [41] improves dramatically. As depicted in Fig. 15(b), the quantum well provides allowed states that substantially narrow the energy distribution of the tunneling electrons, resulting in a sharper turn-on and higher gain.

The predicted performance is for an  $f_{\max}$  of 3.8 THz at a power output per device of  $\sim 1$  mW. In addition to the potential for tremendous performance, the devices can be made using standard fabrication facilities and materials. Because the metal–insulator technology depends on thin vertical

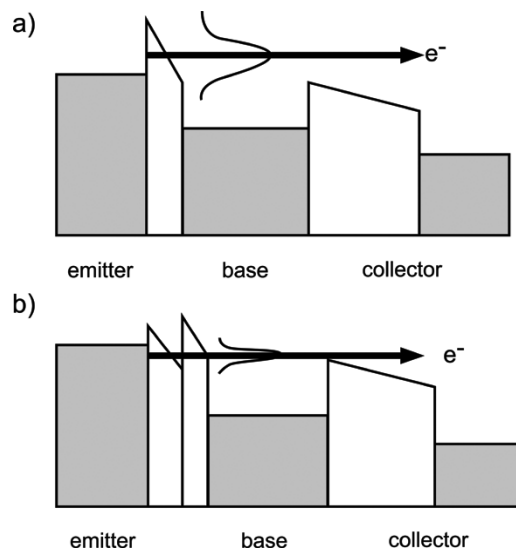


Fig. 15. Concept of a MIMIM tunneling transistor.

dimensions, performance is not expected to degrade significantly when deposited on flexible substrates and over large areas. However, there are numerous material engineering challenges to be overcome in any thin-film technology. In addition, parasitic elements of large macroelectronic devices will need to be understood and their impact included in device models. Current efforts are directed at developing the required materials and deposition technology to provide the desired thin-film structure. Subsequent work will characterize the device performance and reliability.

#### IV. MANUFACTURING

The growing interest in high-performance, large area, low-cost electronic devices and systems fabricated on flexible substrates requires new process tools and methods. Conventional approaches do not allow for rugged, lightweight, flexible, large area macroelectronic circuits incorporating high-mobility transistors. Technologies to provide this capability are under development in three major areas: enhanced TFTs and novel, nanomaterial-based devices as described above, process technologies compatible with large area, flexible, and low temperature substrates, and patterning technologies that can provide micrometer-scale features and alignments over a variety of substrate types and sizes. A major reason for the interest in macroelectronic circuits with the critical dimensions in the 1–10- $\mu\text{m}$  range is that they can be made using processing methods which do not require the complex, costly methods associated with microelectronics. However, for such circuits to become useful, they have to be built on large substrates ( $10^3$  cm<sup>2</sup> to several square meters). This is now being done in production for AMLCDs on glass, as shown in Fig. 16. Thus, there is an existing proof that electronics manufacturing over a large area can be done cost effectively.

Flexible, large area electronics will be most successful when similar capability exists for plastic substrates.

Macroelectronics will ideally benefit from the large investment in manufacturing infrastructure being made by

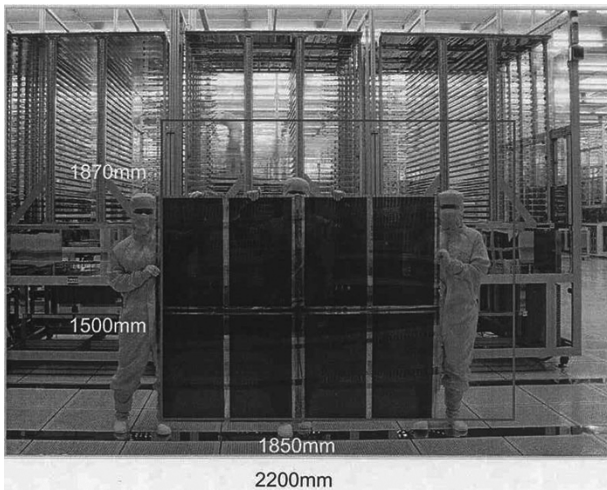


Fig. 16. Seventh-generation (Gen 7) AMLCD glass substrates.

the display and photovoltaic industries. Such methods as sequential lateral solidification and rapid thermal processing are expected to be applicable to large area electronics as well. The method of choice for fabrication of these electronic components is “roll-to-roll” because of the assumed compatibility with flexible substrates and low cost. However, there are considerable challenges to be overcome. The main issues to be addressed are covered well by Sheats [42]. Other manufacturing related topics are also discussed in these PROCEEDINGS (see papers by K. Allen, R. Parashkov, M. Chabinyk, K. Jain, and R. Ludwig).

In order to fully exploit the high mobility performance of the semiconductors developed in the macroelectronics effort, it is necessary to perform lithography with micrometer-scale critical dimensions and registration tolerances. However, large area patterning with high resolution is a significant challenge. In addition to standard photolithography, large area soft lithography techniques that permit micrometer-scale critical dimensions and registration tolerances, as well as high-resolution embossing and delamination methods will be evaluated. The emphasis here is not to develop new approaches as much as to exploit those capabilities being created by the microelectronics and display industries and adapt where necessary for those aspects of the macroelectronics program that are unique.

Direct writing techniques may have more of a role for custom, large area electronics than would be possible for low-cost, high-volume manufacturing [43]–[45]. Direct writing techniques could provide cost-effective, rapid response fabrication of custom, low-volume special purpose macroelectronics. Here, methods like ink-jet printing may be especially attractive. Specialized methods such as thermal spray [46] could provide novel methods for metallization and direct deposition of passives such as resistors, capacitors, and antenna patterns. Laser transfer of fully processed chips may also be important to provide critical, high-performance components not available via roll-to-roll processes or to provide faster and more adaptable and cost-effective assembly than is possible via pick and place [47].

Materials are a critical element of almost any new electronics program. However, again other large area electronic applications are the primary driver. Barrier coatings (to prevent degradation from water, oxygen, or sunlight) and dielectrics are not expected at this time to be unique. However, given the desire for significantly higher performance than with conventional TFTs, it may be necessary to develop novel materials and/or fabrication processes for the gate dielectric if performance commensurate with high mobility is to be realized. Substrates are an area where new approaches may be possible because transparency is not an issue. Besides thin metal foils, plastic films capable of withstanding processing temperatures of over 500 °C such as various silicone resins [48] allowing the high performance (and high fabrication temperature) TFT processes to be done directly on the plastic film can be explored. As mentioned previously, textile substrates can also be considered either to provide better manufacturability, lower cost, or ease of integration into wearable structural elements [49], [50].

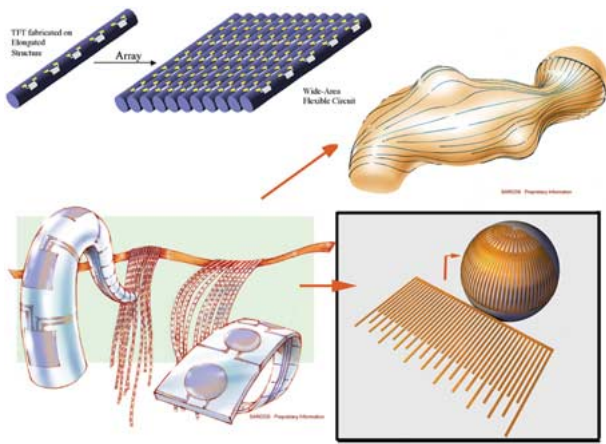
Finally, since one of the main attractions of macroelectronics is “flexibility,” a major issue that must be resolved is just what is meant and how might it be achieved. No doubt there are some applications where a rigid substrate (such as today’s flat panel displays) is adequate. In other situations, a bendable or conformable substrate might be adequate, in others, rollable. At the far end of the spectrum, the flexible electronics might actually be crumpled. Currently, the major efforts in flexible electronics are addressing performance and reliability. However, some promising work has been reported on stretchable interconnects by Wagner [51].

The program is developing new approaches to electrically and mechanically interconnect flexible elongated body structures that contain microelectronic elements to form systems that can be installed over large surface areas with complex geometrical characteristics, such as compounded radii of curvature, or that can be rolled or folded for transportation and which can be rapidly deployed for use in the field.

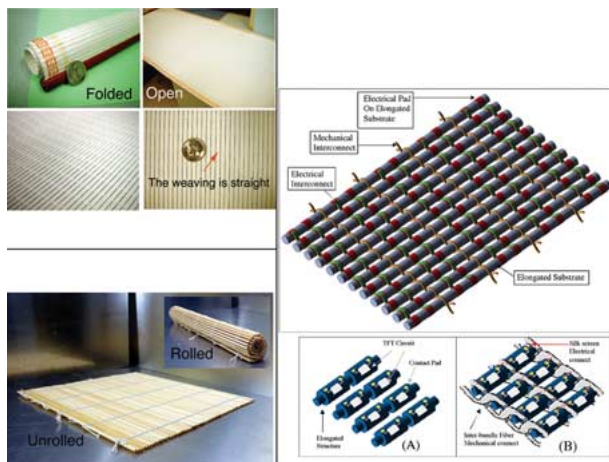
Two of the approaches currently being developed are schematically illustrated in Figs. 17 and 18. In each case, passive and active electronic components such as conductors, resistors, TFTs, and others are fabricated on elongated prismatic substrates such as thin and narrow strips and circular cross section filaments, and the latter are assembled to form large prismatic integrated networks (PINs).

In the approach illustrated in Fig. 17, referred to as PIN on BUS, microelectronic circuits are fabricated on elongated substrates, which are in turn connected to a single or multiple electrical bus. The dimensions of the individual prismatic substrates are adjusted to achieve the desired area coverage once installed on the targeted structure (e.g., airfoil) and also to ensure that physical integrity and device performance are maintained.

In the approach shown in Fig. 18, the elongated prismatic structures are woven together and electrically interconnected to form large area networks containing optoelectronics devices, sensing and actuating elements, power sources, and others, and which can readily be rolled or folded, even in



**Fig. 17.** Schematic diagram illustrating how flexible elongated prismatic elements, such as thin strip or filaments having predetermined dimensions may be connected to a flexible bus and mounted on complex surfaces.



**Fig. 18.** Photographs (top and bottom left) illustrating how rectangular cross section strips and circular section rods may be woven and interconnected to form large area structures that may be rolled or folded. A schematic diagram how the elongated structure may be assembled is shown on the right.

cases where the individual strips or filaments have relatively low flexibility.

## V. CONCLUSION

Macroelectronics has the potential to open new directions in electronics: directions not based on ever-higher levels of integration and performance, but on fulfilling roles that conventional microelectronics cannot. In other papers in these PROCEEDINGS, the case is made for “plastic electronics” that seeks to apply low-cost, roll-to-roll type processing to make simple, inexpensive, “throwaway” electronics. This is one example of a new dimension. In this paper, we have described another dimension—once again, not based on replacing microelectronics (perhaps even exploiting it where appropriate), but on providing a capability that microelectronics is not suited for. Specifically, macroelectronics hopes to provide solutions to problems that require the electronics to be physically large and interconnected such that an entire

area and not just discrete points can be monitored, measured, and modified as needed.

The success of the flat panel display industry and the rapidly developing photovoltaic industry are testaments to the need for large area electronics solutions. However, there are needs that go far beyond these existing technologies. Conformal and flexible form factors to provide portability and ability to install the large area electronics in a variety of locations and form factors is one very desirable attribute that is receiving much attention and is proving to be quite difficult. Even more difficult is to not just integrate a flexible substrate, but also to maintain or even improve electrical performance. It is this capability that we have stressed herein. We have described a variety of challenging application drivers such as RF sensor arrays and physical integrity monitors, but once capability for these types of applications becomes available, then commercial applications will likely follow (for example, “systems on a display panel”).

The keys to achieving the desired levels of functionality are advances in device technology that can be manufactured cost effectively over large areas and process methods that provide these high-performance devices and their interconnections at adequate levels of integration in high yield on flexible substrates with tools that can be operated at reasonable throughput/cost. Much of the required advances in process and tools will come from the display and photovoltaic industry. But to achieve the device/circuit performance for demanding applications, significant improvement in materials and device characteristics must be achieved.

We have described several potential routes to enhanced device performance. These include further refinements of the existing polysilicon TFT technology to improve both device characteristics and uniformity and to achieve modest RF performance. Better understanding of the crystallization process and the effects of defects on alternative semiconductors may lead to integration of materials that can provide significant improvement over today’s TFTs. However, given the difficulty of understanding and overcoming defects in semiconductors, entirely alternative approaches are also being pursued. Rather than try to minimize the impact of defects, certain defect-tolerant and nanostructured semiconductors and CNT-based TFT technology seek to avoid the effects of defects rather than the presence of them. Finally, an even more novel idea is to not use semiconductors at all. Rather, build devices that can operate with high performance, but with amorphous materials (which are the most compatible with low temperature, high throughput, large area processing). To achieve this capability, devices based on MIM diode concepts are being pursued.

It is much too early to know which, if any, of these new concepts can be brought to fruition. But, as this paper and these PROCEEDINGS show, there are strong driving forces to create macroelectronics. So, while microelectronics and now nanoelectronics continue on the road to smaller and smaller, there are also many in the electronics community pushing the idea that “bigger can be better.”

## ACKNOWLEDGMENT

The authors would like to thank M. Lucas of Northrop Grumman, experts at the U.S. Air Force Research Laboratory, U.S. Army Research Laboratory, and CERDEC, P. Williams of System Planning Corporation, and V. Greanya and F. Farzad of Booz Allen Hamilton. The authors would also like to thank D. Van Buren at JPL for the discussions on applications of macroelectronics to space-based optical systems and E. Brandon from JPL for Fig. 7.

## REFERENCES

- [1] V. Lumelsky, M. Shur, and S. Wagner, "Sensitive skin," *IEEE Sensors J.*, vol. 1, no. 1, pp. 41–51, Jun. 2001.
- [2] "Global earthquake satellite system: A 20-year plan to enable earthquake prediction," Jet Propulsion Lab., Pasadena, CA, Doc. 400-1069, Mar. 2003.
- [3] S. N. Madsen, W. N. Edelman, L. J. DiDomenico, and J. LaBrecque, "A geosynchronous synthetic aperture radar for tectonic mapping, disaster management and measurements of vegetation and soil moisture," in *Proc. IEEE Symp. Geoscience and Remote Sensing (IGARSS '01)*, pp. 447–449.
- [4] J. Huang, J. Lou, J. Faria, and J. Kim, "An inflatable L-band microstrip SAR array," in *Proc. IEEE AP-S/URSI Symp.*, 1998, pp. 2100–2103.
- [5] C. W. Chen and A. Moussessian, "MEO SAR system concepts and technologies for earth remote sensing," presented at the AIAA Space Conf., San Diego, CA, 2004.
- [6] W. Edelman, S. Madsen, A. Moussessian, and C. Chen, "Concepts and technologies for synthetic aperture radar from MEO and geosynchronous orbits," presented at the SPIE Int. Asia-Pacific Symp. Remote Sensing of the Atmosphere, Environment, and Space, Honolulu, HI, 2004.
- [7] A. Moussessian, L. Del Castillo, W. Edelman, T. Hatake, J. Huang, S. Madsen, A. Paris, G. Sadowy, and A. Shapiro, "T/R membranes for large aperture scanning arrays," presented at the Earth Science Technology Conf., Adelphi, MD, 2003.
- [8] K. J. Kennedy and C. M. Adams, "International Space Station (ISS) TransHab: An inflatable habitat," in *Proc. 7th Int. Conf. Exposition Engineering, Construction, Operations, and Business in Space*, S. Johnson, K. Chua, R. Galloway, and P. Richter, Eds., 2000, pp. 89–100.
- [9] C.-H. Lee, A. Sazonov, and A. Nathan, "High electron mobility ( $\sim 150 \text{ cm}^2/\text{Vs}$ ) PECVD nanocrystalline silicon top-gate TFT's at 260 °C," presented at the Materials Res. Soc. Spring Meeting, Sec. A, San Francisco, CA, 2005, Paper A17.5.
- [10] R. A. Street, Ed., *Technology and Applications of Amorphous Silicon*. Berlin, Germany: Springer-Verlag, 1999.
- [11] Y. Kuo, Ed., *Thin Film Transistors: Materials and Processes, Amorphous Silicon Thin Film Transistors, Polycrystalline Silicon Thin Transistors*. New York: Kluwer, 2004.
- [12] T. Afentakis, M. Hatalis, T. Voutsas, and J. Hartzell, "Display driver circuits fabricated on flexible stainless steel foils," in *SID Dig.*, vol. 37, 2004, pp. 14–17.
- [13] ———, "High performance polysilicon circuits on thin metal foils," *Proc. SPIE*, vol. 5004, pp. 122–126, 2003.
- [14] T. Afentakis and M. Hatalis, "High performance polysilicon thin film transistor circuits on flexible stainless steel foils," in *Materials Res. Soc. Symp. Proc.*, vol. 769, 2003, pp. 47–52.
- [15] M. Troccoli, T. Afentakis, M. Hatalis, A. Voutsas, M. Adachi, and J. Hartzell, "AMOLED TFT pixel circuitry for flexible displays on metal foils," in *Materials Res. Soc. Symp. Proc.*, vol. 769, 2003, pp. 93–99.
- [16] R. S. Sposili and J. S. Im, "Sequential lateral solidification of thin silicon films on SiO<sub>2</sub>," *Appl. Phys. Lett.*, vol. 69, pp. 2864–2866, 1996.
- [17] H. J. Kim and J. S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin-film transistors," *Appl. Phys. Lett.*, vol. 68, pp. 1513–1514, 1996.
- [18] C.-W. Kim and K.-C. Park, "Development of SLS based SOG display," presented at the Int. Display Manufacturing Conf., Taipei, Taiwan, R.O.C., 2005.
- [19] A. B. Limanov, P. C. van der Wilt, J. Choi, N. Maley, J. Lee, J. R. Abelson, M. G. Kane, A. H. Firester, and J. S. Im, "Sequential lateral solidification of Si films on polymer substrates," in *Int. Display Manufacturing Conf.*, Taipei, Taiwan, R.O.C., 2005.
- [20] M. G. Kane and A. H. Firester, "Macroelectronics: high-performance semiconductor technology on large-area flexible substrates," presented at the USDC Flexible Microelectronics and Displays Conf., Phoenix, AZ, 2005.
- [21] F. Greuter and G. Blatter, "Electrical properties of grain boundaries in polycrystalline compound semiconductors," *Semicond. Sci. Technol.*, vol. 5, pp. 111–137, 1990.
- [22] J. J. J. Yang, P. D. Dapkus, R. D. Dupuis, and R. D. Yingling, "Electrical properties of polycrystalline GaAs films," *J. Appl. Phys.*, vol. 51, p. 3794, 1980.
- [23] H. H. Wieder, "Perspectives on III-V compound MIS structures," *J. Vac. Sci. Technol.*, vol. 15, no. 4, pp. 1498–1506, Jul. 1978.
- [24] L. Canali, J. W. G. Wildoer, O. Kerkhof, and L. P. Kouwenhove, "Low-temperature STM on InAs(110) accumulation surfaces," *Appl. Phys. A.*, vol. 66, pp. S113–S116, Mar. 1998.
- [25] H. H. Wieder, "Surface and interface barriers of In<sub>x</sub>Ga<sub>1-x</sub>As binary and ternary alloys," *J. Vac. Sci. Technol. B*, vol. 21, no. 4, pp. 1915–1919, 2003.
- [26] K. Brennan and K. Hess, "High-field transport in GaAs, InP, and InAs," *Solid State Electron.*, vol. 27, pp. 347–357, 1984.
- [27] D. Scott, M. Urteaga, N. Parthasarathy, J. H. English, and M. Rodwell, "Molecular beam deposition of low-resistance polycrystalline InAs," presented at the Lester Eastman Conf., Newark, DE, 2002.
- [28] H. E. Künig, "Analysis of an InAs thin film transistor," *Solid-State Electron.*, vol. 11, pp. 335–342, 1968.
- [29] E. Menard, K. J. Lee, D. Y. Khang, R. G. Nuzzo, and J. A. Rogers, "A printable form of silicon for high performance thin film transistors on plastic," *Appl. Phys. Lett.*, vol. 84, no. 26, pp. 5398–5400, 2004.
- [30] E. Menard, R. G. Nuzzo, and J. A. Rogers, "Bendable single crystal silicon thin film transistors formed by printing on plastic substrates," *Appl. Phys. Lett.*, vol. 86, pp. 093 507-1–093 507-3, 2005.
- [31] Y. Sun and J. A. Rogers, "Fabricating semiconductor nano/microwires and transfer printing ordered arrays of them onto plastic substrates," *Nano Lett.*, vol. 4, no. 10, pp. 1953–1959, 2004.
- [32] K. J. Lee, M. J. Motala, M. A. Meitl, W. R. Childs, E. Menard, A. Shim, J. A. Rogers, and R. G. Nuzzo, "Large area selective transfer of microstructured silicon: A printing based approach to high performance thin film transistors supported on flexible substrates," *Adv. Mater.*, 2005, to be published.
- [33] Z.-T. Zhu, E. Menard, K. Hurley, R. G. Nuzzo, and J. A. Rogers, "Spin on dopants for high-performance single-crystal silicon transistors on flexible plastic substrates," *Appl. Phys. Lett.*, vol. 86, pp. 133 507-1–133 507-3, 2005.
- [34] M. A. Meitl, Y. X. Zhou, A. Gaur, S. Jeon, M. L. Usrey, M. S. Strano, and J. A. Rogers, "Solution casting and transfer printing single-walled carbon nanotube films," *Nano Lett.*, vol. 4, pp. 1643–1647, 2004.
- [35] E. S. Snow, P. M. Campbell, and J. P. Novak, "High-mobility carbon nanotube thin-film transistors on a polymeric substrate," *Appl. Phys. Lett.*, vol. 86, pp. 033 105-1–033 105-3, 2005.
- [36] Y. Zhou, A. Gaur, S.-H. Hur, C. Kocabas, M. Meitl, M. Shim, and J. A. Rogers, "p-channel, n-channel thin film transistors and p-n diodes based on single wall carbon nanotube networks," *Nano Lett.*, vol. 4, no. 10, pp. 2031–2035, 2004.
- [37] C. Kocabas, M. Meitl, A. Gaur, M. Shim, and J. A. Rogers, "Aligned arrays of single walled carbon nanotubes generated from random networks by orientationally selective laser ablation," *Nano Lett.*, vol. 4, no. 12, pp. 2421–2426, 2004.
- [38] C. Kocabas, S. H. Hur, A. Gaur, M. A. Meitl, M. Shim, and J. A. Rogers, "Guided growth of large scale, horizontally aligned arrays of single walled carbon nanotubes and their use in thin film transistors," *Small*, 2005, to be published.
- [39] S. Kumar, J. Murthy, and M. A. Alam, "Percolating conduction in finite nanowire network," *Phys. Rev. Lett.*, 2005, to be published.
- [40] B. J. Eliasson and G. Moddel, "Metal-oxide electron tunneling device for solar energy conversion," U.S. Patent 6 534 784, 2003.
- [41] G. Moddel and B. J. Eliasson, "High speed electron tunneling device and applications," U.S. Patent 6 563 185, 2003.

- [42] J. R. Sheats, "Manufacturing and commercialization issues in organic electronics," *J. Mater. Res.*, vol. 19, no. 7, pp. 1974–1989, 2000.
- [43] A. Piqué and D. B. Chrisey, Eds., *Direct Write Technologies for Rapid Prototyping Applications: Sensors, Electronics, and Integrated Power Sources*. New York: Academic, 2002, p. 726.
- [44] D. B. Chrisey, A. Piqué, R. Mohdi, H. D. Wu, R. C. Y. Auyeung, and H. D. Young, "Direct writing of conformal mesoscopic electronic devices by MAPLE DW," *Appl. Surf. Sci.*, vol. 168, pp. 345–352, 2000.
- [45] K. M. A. Rahman, D. N. Wells, and M. T. Duignan, "Laser direct-write of materials for microelectronics applications," in *Materials Res. Soc. Symp. Proc.*, vol. 624, 2001, pp. 99–105.
- [46] S. Sampath, A. Patel, A. H. Dent, R. Gambino, H. Herman, R. Greenlaw, and E. Tormey, "Thermal spray techniques for fabrication of meso-electronics and sensors," in *Materials Res. Soc. Symp. Proc.*, vol. 624, 2000, p. 181.
- [47] T. D. Sands, W. S. Wong, and N. W. Cheung, "Layer transfer by bonding and laser lift-off," in *Wafer Bonding—Applications and Technology*, M. Alexe and U. Gosele, Eds. Berlin, Germany: Springer-Verlag, 2004.
- [48] M. Suto, N. Kushibiki, and D. Katsoulis, "Film substrates based on silicone resins," presented at the Materials Res. Soc. Spring Meeting Symp. Flexible Electronics Technology, San Francisco, CA, 2004, Paper H9.2.
- [49] D. Marculescu, R. Marculescu, N. H. Zamora, P. Stanley-Marbell, P. K. Khosla, S. Park, S. Jayaraman, S. Jung, C. Luterbacj, W. Weber, T. Kirstein, D. Cottet, J. Grzyb, G. Troster, M. Jones, T. Martin, and Z. Nakad, "Electronic textiles: a platform for pervasive computing," *Proc. IEEE*, vol. 91, no. 12, pp. 1993–1994, Dec. 2003.
- [50] D. J. Sikkema, M. G. Northolt, and B. Pourdeyhi, "Assessment of new high-performance fibers for advanced applications," *MRS Bull.*, vol. 28, no. 8, pp. 579–584, 2003.
- [51] S. P. Lacour, J. Jones, S. Wagner, T. Li, and Z. Suo, "Stretchable interconnects for elastic electronic surfaces," *Proc. IEEE (Special Issue on Flexible Electronics Technology)*, 2005, to be published.

**Robert Reuss** (Senior Member, IEEE) received the Ph.D. degree in chemistry from Drexel University, Philadelphia, PA, in 1971.

Prior to joining DARPA, Dr. Reuss spent twenty years in various technology and research management positions with Motorola. Earlier, he worked for the U.S. government as a research and development manager for seven years and was a Research Faculty member at the University of Colorado for three years, joined the Defense Advanced Research Projects Agency (DARPA) as a Program Manager in the Microsystems Technology Office in August 2001. He is responsible for several research programs including the Macroelectronics, Organic Nanocomposite Potovoltaic, Embedded Configurable Signal Processing, Asynchronous Logic, and Mission Specific Processing programs. Dr. Reuss was elected to Motorola's Science Advisory Board, and is a member of the Electrochemical Society, Materials Research Society, and Society for Information Display, and a Senior Member of IEEE and a past chairman of the Phoenix Chapter of IEEE Waves and Device Societies. He has published over 50 papers and has been awarded 13 U.S. patents. His technology interests lie in the area of application of materials and electrochemistry technologies for advanced microelectronic applications and microsystems integration as well as large area electronics.

**Babu R. Chalamala** (Senior Member, IEEE) received the B.Tech. degree in electronics and communications engineering from Sri Venkateswara University, Tirupati, India, in 1987 and the Ph.D. degree in physics from the University of North Texas, Denton, in 1996.

He was a research staff member at MCNC, Research Triangle Park, NC; Motorola, Tempe, AZ, and Texas Instruments in Dallas for ten years. He also held visiting appointments at SRI International and FOM Institute for Atomic and Molecular Physics in Amsterdam. He is currently the Founder and President of Indocel Technologies, Research Triangle Park, a high-volume manufacturer of portable energy products. He has published 85 technical papers and was awarded eight U.S. patents. His expertise is in field emission displays, vacuum microelectronics, thin films, and microelectronic materials development.

Dr. Chalamala is a Member of the Materials Research Society and the Electrochemical Society. He has played key leadership roles with IEEE Lasers and Electro-Optics Society (LEOS) and Materials Research Society (MRS) for the last ten years. He served on the Technical Council of the IEEE LEOS and was the Chair of the Technical Committee on Displays from 2001 to 2004. He led an IEEE-wide initiative that created the IEEE/OSA JOURNAL OF DISPLAY TECHNOLOGY and currently serves on the Steering Committee of the new journal. He was the Organizer and Chair of three successful MRS symposia on flat panel displays, sensors, and flexible electronics and was selected to serve as a General Chair of the 2006 Materials Research Society Fall Meeting. He was Organizer of the 1st IEEE Workshop on organic LEDs (OLEDs) in 2002 and was a Member of the Organizing Committee of IEEE LEOS annual meetings for the last five years. He served as a Guest Editor of the PROCEEDINGS OF THE IEEE special issue on flat panel display technology in April 2002, the *MRS Bulletin* special issue on microelectronics packaging and integration in January 2003, and the IEEE JOURNAL ON SELECTED TOPICS IN QUANTUM ELECTRONICS special issue on OLEDs in January 2004.

**Alina Moussessian** (Member, IEEE) received the Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1997, where she worked on microwave and millimeter-wave power combining, beam-steering, computer-aided design and microwave circuits.

After graduation, she joined the Radar Science and Engineering Section, Jet Propulsion Laboratory (JPL), Pasadena, where she worked on Shuttle Radar Topography Mission (SRTM) radar testing and the development of a testbed airborne radar sounder for the Europa Orbiter Radar Sounder. She worked in industry from 2000 to 2001, developing optical telecommunication components. Since returning to JPL in 2002, she has been involved in technology development projects for very large aperture phased arrays. She is currently working on membrane radar systems for future NASA missions and advanced components technology for membrane-based phased arrays. She is currently the Supervisor of the Radar Technology and Hardware Implementation Group.

**Michael G. Kane** received the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, in 1994, where he studied ultrafast carrier-carrier scattering among photoexcited nonequilibrium carriers in semiconductors.

He was Project Leader of the Ultrafast All-Optical Switching Project at Siemens Corporate Research, and Group Head of the GaAs IC Design Group at Microwave Semiconductor Corp. He has also served as a Visiting Faculty Member in the Department of Electrical Engineering, Princeton University, teaching courses in solid-state physics and solid-state displays. He is currently a Distinguished Member of the Technical Staff at Sarnoff Corp., Princeton. At Sarnoff, he has worked on novel organic and inorganic thin-film transistor technologies for flexible plastic active matrix displays and electronic circuits, architectures for organic electroluminescent displays, liquid-crystal display pixel structures, electrical instabilities in amorphous and polycrystalline silicon thin-film transistors, SiGe BiCMOS wireless IC design, and optical range camera and monolithic fingerprint imagers. He is the author or coauthor of about 50 technical papers on electronic and optical processes in semiconductors, solid-state displays, optical switching, and electronic circuit design, and holds 13 U.S. patents on analog and digital circuit design, organic electroluminescent displays, plasma displays, and microelectronic fluid delivery.

**Amrita Kumar** received her M.S. and Ph.D. degrees in mechanical engineering and mechanics from Drexel University, Philadelphia, PA, in 1998.

She is Director of Business Development, Projects and Technology at Acellent Technologies Inc., Sunyvale, CA, and has served Acellent in various capacities over the past six years, including being Acellent's liaison with the industry. She specializes in the manufacturing and micromechanical analysis of composite materials and in areas of structural health monitoring. She has authored over 20 publications in journals and conference proceedings and is a member of the 2003 SPIE Smart Structures award-winning team.

Dr. Kumar is the recipient of the Albert and Harriet Soffa Fellowship (1995–1998), a graduate award in recognition of academic achievement and research in mechanical engineering. She serves on several advisory committees, including Caterpillar's SHIELD program.

**David C. Zhang** received double B.S. degrees from the Department of Automation and the School of Economics and Business Management, Tsinghua University, Beijing, China, in 1994 and the M.S. and Ph.D. degrees from the Electrical and Computer Engineering Department, University of Maryland, College Park, in 1999 and 2002, respectively.

He was a Graduate Fellow of the University of Maryland, College Park from 1997 to 1999. He joined Acellent Technologies, Sunyvale, CA, in 2002, and he is currently working on multiple advanced projects from electrical systems design to signal processing in the structural health monitoring (SHM) field. His expertise is in signal processing, optimization, and electronics and electrical systems design.

Dr. Zhang received the Outstanding Graduate honor when he graduated in 1994.

**John A. Rogers** received the B.A. and B.S. degrees in chemistry and in physics from the University of Texas, Austin, in 1989 and the S.M. degrees in physics and in chemistry and the Ph.D. degree in physical chemistry from the Massachusetts Institute of Technology, Cambridge, in 1992 and 1995, respectively.

From 1995 to 1997, Rogers was a Junior Fellow in the Harvard University Society of Fellows. During this time he also cofounded and served as Director of a thin-film metrology startup that was later acquired by an established company in 1998. He joined Bell Laboratories as a Member of Technical Staff in the Condensed Matter Physics Research Department in Fall 1997. He served as Director of this department from 2000–2002. He is currently Founder Professor of Engineering at the University of Illinois, Urbana-Champaign, where he pursues research on flexible electronics, unusual photonic systems, and new methods for micro/nanofabrication.

**Miltos Hatalis** (Senior Member, IEEE) received the B.S. degree in physics from Aristotle University, Thessaloniki, Greece, in 1982, the M.S. degree in electrical and computer engineering from the State University of New York, Buffalo, in 1984, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, in 1987.

He joined the Department of Electrical and Computer Engineering of Lehigh University, Bethlehem, PA, in 1987 as an Assistant Professor. He was promoted to Associate in 1991 and to Professor in 1995. In 1992, he was also a Visiting Scientist at Xerox Palo Alto Research Center. He is the author or coauthor of over 150 technical publications on polysilicon thin-film transistor technology, including two book chapters. His research interests are on electronic thin-film materials, devices and circuits for flat panel displays, and integrated microsystems on a variety of substrates, including silicon, glass, flexible metal foils, or plastic substrates.

Dr. Hatalis has served as Chairman of the organization committee for five technical workshops and conferences related to flat panel displays.

**Dorota Temple** received the Ph.D. degree in solid-state physics from the AGH University of Science and Technology, Cracow, Poland.

She is the Director of Electronic Materials and Microstructures in the Center for Materials and Electronic Technologies of RTI International, Research Triangle Park, NC. She has over 15 years of experience in the development of materials and processes for ICs, displays, and sensors. She has authored over 100 publications and holds six U.S. patents.

**Garret Model** received the B.S.E.E. degree from Stanford University, Stanford, CA and the M.S. and Ph.D. degrees in applied physics from Harvard University, Cambridge, MA.

He spent the first four years of his professional career as a founding employee at a Silicon Valley solar cell start-up company. He recently took a three-year leave of absence from his position as a professor of Electrical Engineering at the University of Colorado, Boulder, to cofound Phiar Corporation, Boulder, where he serves as President and CEO. Phiar develops ultra-high-speed metal-insulator electronic devices. He is an inventor on over 20 U.S. patents and has coauthored over 120 technical publications.

Dr. Model is a Fellow of the Optical Society of America.

**Blake Eliasson** received the B.S.E.E. degree from Montana State University, Bozeman, in 1995 and the M.S. degree in electrical engineering and the Ph.D. degree from the University of Colorado, Boulder, in 1997 and 2001, respectively.

He is a Cofounder and Director of Engineering of Phiar Corporation, Boulder, where he directs device development and carries out design and analysis of the tunnel junction devices that form the core of Phiar's technology. At the University of Colorado, he developed the metal-insulator-insulator-metal (MIIM) diode as part of his thesis work on antenna-coupled MIM and MIIM detectors for solar energy conversion. He holds two patents and is a named inventor on three additional patents and one allowed patent application.

**Michael J. Estes** received the Ph.D. degree in electrical engineering from the University of Colorado, Boulder, in 1995.

From 1986 to 2001, he served as a research and development officer in the U.S. Air Force and worked on such projects as gallium nitride ultraviolet photodetectors, light emission from nanostructured silicon, optical nonlinearities in silica glass, and atmospheric lidar sensors. From 2001 to 2004, he was a Cofounder and Product Development Engineer at Phiar Corporation. He is currently a Senior Electro-Optic Engineer at Melles Griot Electro-Optics Division, Longmont, CO, where he develops diode laser products. His technical interests include optoelectronic materials and devices, particularly plasmonic devices.

**Joseph Kunze** received the B.S. degree in mechanical engineering from Worcester Polytechnic Institute, Worcester, MA, in 1988 and the M.S. degree in mechanical and aerospace engineering and the Ph.D. degree in materials science and engineering from the University of Virginia, Charlottesville, in 1991 and 1996, respectively.

Prior to launching SI2 Technologies Inc. from Triton Systems, Inc., he was the Vice President and Business Unit Leader of Triton's Structural Materials Group. He is currently President of SI2 Technologies Inc., Chelmsford, MA, where he leads a team of highly trained and experienced personnel and industry leading consultants. He has successfully managed a number of government contract development programs with a focus on transitioning and implementing the technology into military and commercial applications. His efforts led to the Direct Write electronics material and process technology, which became one of the core underpinnings of SI2's business. He led an effort that developed a modified silver ink for use in Direct Write manufacturing. He also designed Triton's first organic FETs for manufacture using Direct Write processes. His technical activities are focused on developing and commercializing multifunctional electronic structures and on how to take a "dumb" structure and make it "smart" by adding lightweight, conformal sensors.

**Erik S. Handy** received the Ph.D. degree from the Massachusetts Institute of Technology, Cambridge, MA, in 1999, where his graduate research focused on the development of metal-organic LEDs.

He laid the technical foundation for Sensera, Inc., a Triton Systems' spin-off company focused on sensor development. He served as Principal Investigator (PI) for a number of programs. This technology became the basis for establishing another venture-backed company, Triton BioSystems, Inc. He is currently is a Senior Scientist at SI2 Technologies Inc., Chelmsford, MA, where he is responsible for materials and manufacturing issues relating to the design, fabrication, and testing of conformal sensor systems. His work ranges from the fundamental development of SI2's Direct Write materials and manufacturing technology to the application of the technology in the design and fabrication of conformal antennas and associated microelectronics. He conceived and led the development of SI2's proprietary laser transfer Direct Write processes for high-performance electronics manufacture. He has been PI on various programs, including efforts using laser transfer to build conformal transmit/receive (T/R) modules for antenna systems and efforts to develop conformal radar antennas for small unmanned aerial vehicles (UAVs). Several patents have been filed related to his work at SI2 Technologies and Triton BioSystems.

**Eric S. Harmon** received the B.S. degree in electrical engineering from the University of California, Davis, in 1989 and the M.S.E.E. and Ph.D. degrees in solid-state physics from the Electrical Engineering Department, Purdue University, West Lafayette, IN, in 1990 and 1994, respectively.

He is Research Manager at LightSpin Technologies Inc., Norfolk, MA. He has commercialized a 40-GHz optical detector module and is currently developing single-photon sensitive photodetectors and multigigahertz thin-film transistors. His past work has measured minority carrier transport properties in heavily doped GaAs and InGaAs, thermal velocity limits to diffusion in bipolar transistors, and mechanisms of ultrafast recombination in LTG-GaAs. His current research focuses on compound semiconductor devices and materials, notably optoelectronic devices, high-speed transistors, and defect-tolerant thin-film devices.

**David B. Salzman** received the B.S. degree in physics from Yale University, New Haven, CT, and the M.A. and Ph.D. degrees in physics from the University of Chicago, Chicago, IL.

He has served as a Program Officer in advanced scientific computing at the National Science Foundation, where he created the 44-agency government-wide initiative on scientific visualization; as the executive director for research of the John von Neumann National Supercomputer Center, with an appointment in applied and computational mathematics at Princeton University; as resident technologist for the strategic computing and telecommunications program at Harvard University; and in technical and management positions at startup companies prior to LightSpin Technologies, Inc. He is currently President and Co-founder of LightSpin Technologies Inc., Bethesda, MD. He has published papers and invented in the fields of semiconductors, computer graphics, and electron optics.

**Jerry M. Woodall** (Fellow, IEEE) received the B.S. degree in metallurgy from the Massachusetts Institute of Technology, Cambridge, MA, and the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY.

He is a Distinguished Professor at Purdue University, West Lafayette, IN, and serves as Chief Scientist of LightSpin Technologies, Inc. He created the first high-purity bulk crystals of GaAs, the first practical compound semiconductor heterojunction, GaAs/AlGaAs, (making continuous-wave lasers possible), and pioneered its derivatives, e.g., high-efficiency red LEDs, the superluminescent IR LED, the heterojunction bipolar transistor (HBT) and pseudomorphic high electron mobility transistor (p-HEMT, used in RF and microwave circuits), the weight-efficient solar cell, and low-temperature molecular beam epitaxy (MBE) growth. He has published 334 publications in the open literature and has been issued 67 U.S. patents.

Dr. Woodall is a National Medal of Technology (NMT) Laureate. His NMT citation attributes fully half of the entire world's annual sales of compound semiconductor components to his research legacy. He is a Member of the National Academy of Engineering (NAE); a Fellow of the American Physical Society (APS), the Electrochemical Society (ECS), and the American Vacuum Society (AVS); and Past President of the ECS and AVS. Included among his awards are the IEEE Jack Morton Award, the ECS Solid State Science and Technology Award, the ECS Founder's Award, an IR 100 Award, a Heinrich Welker Gold Medal, the AVS Founder's Award, and an IEEE Third Millennium Award.

**M. Ashraf Alam** received the B.S.E.E. degree in electrical engineering from Bangladesh University of Engineering and Technology, Dhaka, in 1988, the M.S. degree in electrical engineering from Clarkson University, Potsdam, NY, in 1991, and the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, in 1994.

From 1995 to 2000, he was with Bell Laboratories, Lucent Technologies, Murray Hill, NJ, as a Member of Technical Staff in the Silicon ULSI Research Department. From 2001 to 2003, he was the Technical Manager of the IC Reliability Group at Agere Systems, Murray Hill, NJ. In 2004, he joined Purdue University as a Faculty Member in the Electrical and Computer Engineering Department. His research interest involves the physics of carrier transport in semiconductor devices, and he has worked on the theory of transport models, quasi-ballistic transport in bipolar transistors, metal-organic chemical vapor deposition (MOCVD) crystal growth, laser dynamics, and most recently, on the theory of oxide reliability and transport in nanocomposite materials.

**Jayathi Y. Murthy** received the Ph.D. degree from the Department of Mechanical Engineering, University of Minnesota, Minneapolis, in 1984.

She has worked in both academia and industry. She spent over ten years at Fluent Inc., a leading developer and vendor of computational fluid dynamics (CFD) software. She moved to Carnegie Mellon University in 1998 as Associate Professor in the Department of Mechanical Engineering. Since 2001, she has been a Professor in the School of Mechanical Engineering, Purdue University, West Lafayette, IN. She is the author of over 100 technical papers and reports, and two book chapters on numerical methods, and has edited two volumes on heat transfer and CFD. She is an Editor of the second edition of the *Handbook of Numerical Heat Transfer* (New York: Wiley, 2004) and serves on the Editorial Board of *Numerical Heat Transfer*. Her research interests lie in the computational heat transfer and fluid mechanics, with an emphasis on the development of unstructured, solution-adaptive finite volume methods for industrial applications. More recently, her work has focused on the analysis of microscale heat transfer, particularly in emerging microelectronics applications.

Prof. Murthy serves on the K-16 and K-20 committees of the American Society of Mechanical Engineers (ASME).

**Stephen C. Jacobsen** received the B.S. and M.S. degrees from the University of Utah, Salt Lake City, in 1967 and 1970, respectively, and the Ph.D. degree from the Massachusetts Institute of Technology, Cambridge, in 1973.

He returned to Utah to establish the Center for Engineering Design (CED), Salt Lake City, where he is currently Director and a Professor of Mechanical Engineering. He holds additional appointments in the Bioengineering, Computer Science, and Surgery Departments at the University of Utah. He founded Sarcos Research Corporation (SRC) and is the President and Chairman of the Board. He has been a key innovative influence in CED and SRC activities, which include: 1) biomedical systems—high-performance prosthetic limbs, iontophoretic drug delivery systems, artificial kidneys, and peritoneal access implants; 2) dexterous robots; 3) entertainment robots; 4) teleoperation systems; and 5) microelectromechanical systems (MEMS). He is currently Principal Investigator (PI) of projects focused on the development of new compact thermochemical hydraulic actuator for legged robots, and PI on the Defense Advanced Research Projects Agency (DARPA)-funded EHPA and WEAR EXO projects. He currently holds over 150 U.S. and foreign patents, and has authored over 157 publications.

Dr. Jacobsen is a Member of the National Academy of Engineering and the National Institute of Medicine. He has received numerous awards for system design and innovation.

**Marc Olivier** received the Ph.D. degree in physics from McGill University, Montreal, QC, Canada, in 1985.

He has acted as Program Manager of the microelectromechanical systems (MEMS) group at Sarcos Research Corporation, Salt Lake City, UT, and is currently Vice-President of Advanced Systems. His background is in technical, engineering, and scientific R&D and project management. He has been involved in the development of devices and systems, and research work including: 1) MEMS ranging from fluid pressure sensors to electrostatic levitated structures for multiaxis accelerometers; 2) multiaxis, force-moment sensors for legged robots; 3) miniature vacuum pumps for handheld chemical and biological sensors; 4) compact, high power density actuators that use high energy density fuels and tailored for legged robots; 5) ambulatory robots for the Defense Advanced Research Projects Agency (DARPA) WEAR project (Co-Principal Investigator, ongoing project); 6) electromagnetically levitated robots (system used on the Priroda module of the space station); and 7) several systems for biological research, crystal growth, and laser material processing in space.

**David Markus** received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree in biomedical engineering from the University of Minnesota, Minneapolis.

He was a BioMEMS Postdoctoral Research Associate in the Department of Electrical and Computer Engineering, University of Minnesota. He is currently with Sarcos Research Corporation, Salt Lake City, UT. His current research focus on the development of three-dimensional microinterconnection methods for microelectromechanical systems (MEMS) and microelectronics. He has specialized in the area of MEMS/bioMEMS for ten years. His MEMS/bioMEMS research activities included: 1) smart phacoemulsification and automatic intraocular lens (IOL) delivery system; 2) piezoelectric inertial biosensors; 3) piezoelectric inchworm motor for Rocky 7 MARS Rover NMR detector; 4) surface micromachined piezoelectric vibration, acoustic, and pressure sensors for aircraft health monitoring system; 5) rapid polymerase chain reaction (PCR) instrumentation; 6) integrated piezoresistive pressure sensor and submicrometer filter for implantable glucose sensor; 7) microoptic probe for root canal surgery; and 8) automatic microoptic and laser probe for orthopedic surgery.

**Paul M. Campbell** received the Ph.D. degree in physics from Pennsylvania State University, University Park, in 1980.

He worked for five years as a physicist at the General Electric Corporate Research and Development Center, Schenectady, NY, where he investigated novel compound semiconductor materials, processes, and devices. In 1985, he joined the Electronics Science and Technology Division of the Naval Research Laboratory, Washington, DC, as a Research Physicist, where for the last 20 years he has pursued research in the growth, fabrication, and measurement of the transport and optical properties of compound semiconductor heterostructures, the fabrication of nanostructures using proximal probes such as the atomic force microscope, and most recently the extraordinary properties and possible intriguing applications of carbon nanotubes. As the author of approximately 100 journal papers and invited talks, he contributes frequently to the scientific literature and occasionally to its proliferation.

**Eric Snow** received the Ph.D. degree in physics from the University of North Carolina, Chapel Hill, in 1986.

Following the completion of his degree, he was a National Research Council Postdoctoral Fellow at the Naval Research Laboratory (NRL), Washington, DC. He became a member of the full-time staff in the Electronics Science and Technology Division at NRL in 1987. Since 1998, he has been Head of the NRL Nanotechnology Section. Currently, his research is focused on the electronic and sensor applications of carbon nanotubes.