

Three-dimensional silicon integration

Three-dimensional (3D) silicon integration of active devices with through-silicon vias (TSVs), thinned silicon, and silicon-to-silicon fine-pitch interconnections offers many product benefits. Advantages of these emerging 3D silicon integration technologies can include the following: power efficiency, performance enhancements, significant product miniaturization, cost reduction, and modular design for improved time to market. IBM research activities are aimed at providing design rules, structures, and processes that make 3D technology manufacturable for chips used in actual products on the basis of data from test-vehicle (i.e., prototype) design, fabrication, and characterization demonstrations. Three-dimensional integration can be applied to a wide range of interconnection densities ($<10^4/\text{cm}^2$ to $10^8/\text{cm}^2$), requiring new architectures for product optimization and multiple options for fabrication. Demonstration test structures, which are designed, fabricated, and characterized, are used to generate experimental data, establish models and design guidelines, and help define processes for future product consideration. This paper 1) reviews technology integration from a historical perspective, 2) describes industry-wide progress in 3D technology with examples of TSV and silicon-silicon interconnection advancement over the last 10 years, 3) highlights 3D technology from IBM, including demonstration test vehicles used to develop ground rules, collect data, and evaluate reliability, and 4) provides examples of 3D emerging industry product applications that could create marketable systems.

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Introduction

Three-dimensional (3D) die stacks and high-bandwidth silicon packaging technology using emerging through-silicon vias (TSVs), thinned silicon, and fine-pitch silicon-silicon interconnections (SSIs) make use of a wide variety of technology structures, materials, and processes. Universities, consortia, and industry have driven research and early demonstrations for a decade. TSV and SSI interconnection density can scale in excess of six orders of magnitude, making the technology widely applicable from simple to very complex applications. At IBM, new 3D test-vehicle (i.e., prototype) designs followed by build, assembly, and characterization studies continue to provide technologists with an understanding of structure

and process-integration capabilities and limitations. Results from these technology studies provide guidance on 3D design rules, structures, processes, tests, and reliability, which can support the manufacturing of products and provide data that we may use to determine technology directions. Practical technology fabrication and integration approaches need to consider targeted TSV and SSI interconnection density, silicon thickness, and power densities. In addition, decisions with respect to options such as TSV conductor material, SSI integration material, and use of die-on-die, die-on-wafer, or wafer-to-wafer process approaches need to be made with regard to interconnection redundancy, die size, yield, cost, and test methodology.

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In 2006 and 2007, interest in 3D technology indicated its growing importance, as observed from industrial press announcements, collaboration through new 3D consortia, growing attendance in technical conferences, increasing patent applications, and increasing technical publications and books. Examples of these press announcements, which include product applications, are presented later in this paper. Perhaps as researchers and industry technologists drive this emerging 3D technology forward into miniaturized products, benefits in power savings, continued system performance scaling (beyond traditional lithographic semiconductor scaling), and lower-cost products can be realized.

In this technical publication, we review advancements in 3D microelectronics, describe the technical progress of 3D microelectronics in universities, consortia, and industries, highlight test structures designed and used at IBM Research, and then describe 3D systems and applications with examples of benefits to products.

3D microelectronics historical evolution

Following the discovery, subsequent understanding, and early manufacture of the transistor from 1947 through the mid-1960s [1–5], Moore predicted a doubling of semiconductor circuit density every 12–18 months [6]. From a die with hundreds of transistors in the 1960s to dies approaching billions (10^9) of circuits in 2008, on-chip integration has continued to require lithographic advancements for circuit and wire density increases through time and has led to increasing the number of wiring levels on the chip. Over decades of semiconductor scaling, on-chip integration has far out-stripped off-chip 3D integration and growth in I/O interconnections. For off-chip interconnections over the last five decades, I/O interconnections grew from tens of I/O interconnections to about several thousands of I/O interconnections for the most complex die manufactured today. **Figure 1(a)** shows 3D technology evolution for silicon chips, packages, and printed wiring boards (PWBs), along with the resulting relative I/O interconnection density for silicon 3D circuits, chip stacking, and silicon packaging, as well as for ceramic and organic packaging [7–21]. It is interesting to note that as new package form factors have entered production (such as thin-film sequential buildup technology on organic packages, thin film on ceramic packages, and wire-bonding chip stacks on organic or ceramic packages), these system-integration solutions have had severe interconnection density limitations that are on the order of thousands of interconnections ($10^3/\text{cm}^2$). When compared to on-chip interconnection densities of hundreds of millions of interconnections ($10^8/\text{cm}^2$), one can understand why on-chip integration has been sought for system integration wherever possible in order to achieve low-cost products. However, as shown

in **Figure 1(b)**, the emerging 3D integration approaches can be implemented with different packaging form factors to combine TSVs, thinned silicon, and SSIs as required to achieve higher interconnection density. For example, high bandwidths may be achieved using 3D chip integration, 3D die stacking, or 3D silicon packaging in which each form factor offers high interconnection density ($10^4/\text{cm}^2$ to $10^8/\text{cm}^2$). Therefore, tradeoffs between best system form factors will be dependent on factors such as system architecture, manufacturing costs, and test and assembly integration yields.

To further understand the evolutionary progression of various package levels shown in Figure 1(b), we consider the following market analysis. The complex integrated circuit (IC) and system implementations that use high-density packaging schemes serve as alternatives to the increasingly expensive system-on-a-chip (SoC) designs. Among these high-density semiconductor packaging solutions that leverage the z-axis dimension of the die, the stacked multichip package and the stacked-die system-in-a-package (SiP) have been available for several years. Most of the technology development in this area was generated mainly in the telecommunications industry for use in handsets, as a response to the demand for smaller, lighter, less-expensive, more-powerful, and energy-efficient ICs. A multichip package holds two or more IC dies in a single package, while an SiP contains combinations of IC dies and active and passive components interconnected to form a complete system or subsystem. More recently, Samsung Electronics announced that it was able to stack 16 NAND flash dies into a single multichip package to support up to 16 GB of flash memory [22].

On the other hand, the package-on-package (PoP) solution has emerged in the mobile phone OEM (original equipment manufacturer) industry as an alternative to SiP, which had presented this industry with various technical challenges (e.g., integration of disparate technologies) and business challenges (e.g., inflexible IC supply choices and integrated product reliability issues) [23]. PoP technology allows the stacking of standard memory and logic packages in the OEM surface-mount assembly flow, electrically interconnecting the packages with solder balls. Another example of the PoP scheme was offered by integrated device manufacturer STMicroelectronics late in 2006 when it introduced the integration of high-density memory (14×14 mm, 152 balls, 0.65-mm ball pitch) with a base-band or application processor for use in high-end wireless handsets [24]. In a variation of the PoP approach, known as package-in-package (PiP), two or more DRAM packages are assembled and overmolded (i.e., encapsulated with a polymer), resulting in a single package.

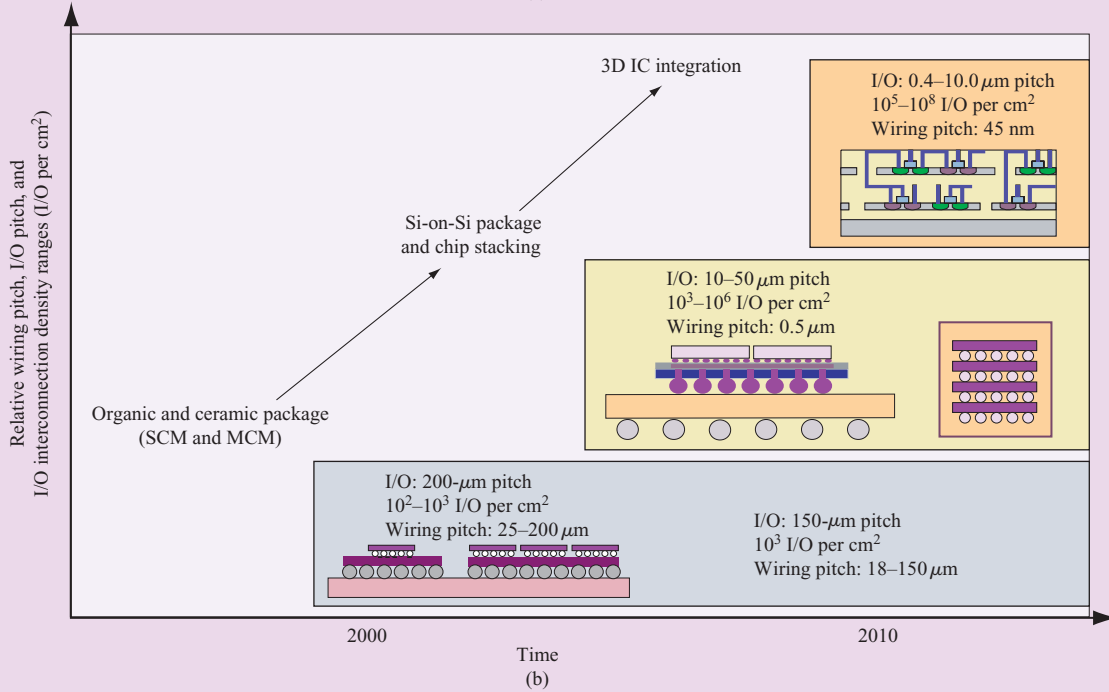
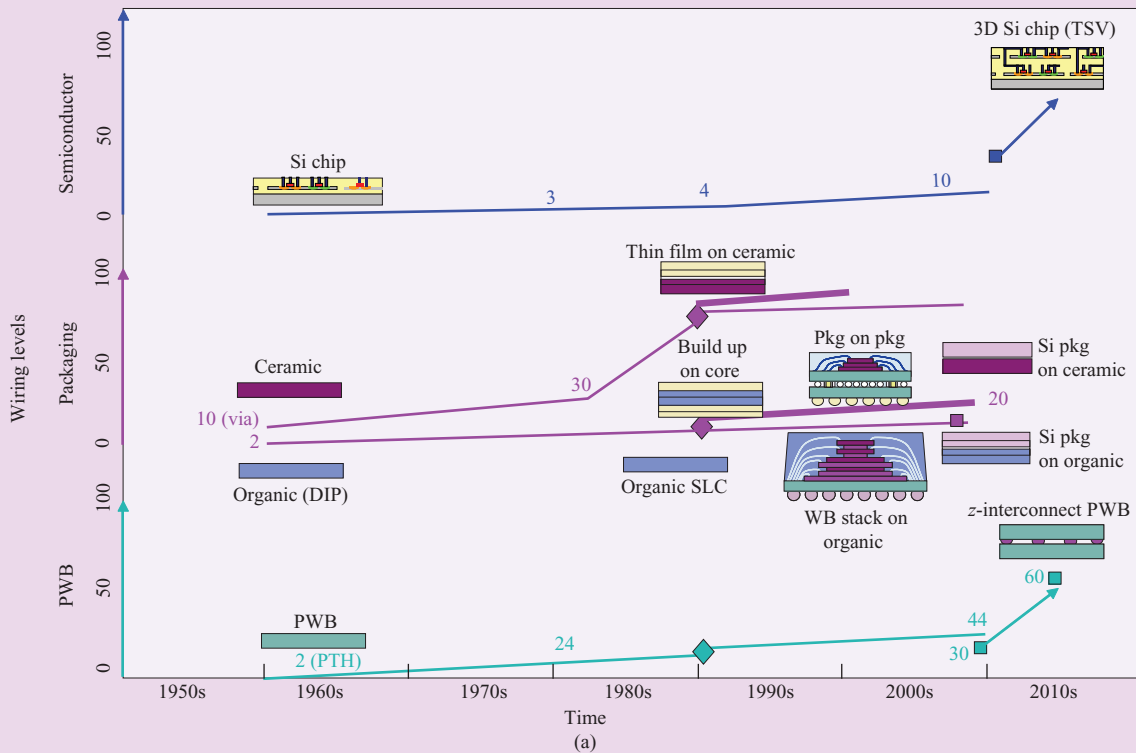


Figure 1

Three-dimensional (3D) microelectronic module history and relative I/O density comparison. (a) Microelectronic industry 3D wiring levels and integration versus time. The y-axis represents density in units of I/O interconnections per cm^3 . (b) Relative comparison of I/O densities for 3D silicon, 3D die stacking, and silicon packaging, for both ceramic and organic packaging. (WB: wire bonding; DIP: dual inline package; SLC: surface laminar circuit; MCM: multichip module; SCM: single-chip module; pkg: package; PTH: plated through-hole.)

Looking toward the future, industry and academic researchers are developing wafer-to-wafer and die-to-wafer stacking techniques for the fabrication of devices that leverage the z -direction but eliminate the need for multiple packages [25]. Additionally, these techniques reduce interconnect delays, form factors, and power consumption while allowing integration of numerous heterogeneous devices. In the wafer-to-wafer approach, circuitry is divided into sections that are built onto separate wafers using standard processing methods. The wafers are then post-processed for through-silicon interconnection, creating the vertical connectors. The wafers are aligned, bonded, thinned, and diced into individual devices. In October 2006, several equipment manufacturers, led by Alcatel, EV Group, Semitool, and XSil, formed a consortium, dubbed EMC-3D, to address the technical and cost issues associated with the creation of TSV interconnect technology for die stacking and wafer-to-wafer attach. In the die-to-wafer variation, a known good die is bonded to a wafer. This approach is preferred in configurations that require three or more dies in a stack. Privately held Ziptronix, Inc., a spin-out business of the Research Triangle Institute, advanced the state of the art in the die-to-wafer methodology when it introduced, late in 2005, a direct bond interconnect technology (a covalent room-temperature bond) that replaces through-die vias, increases electrical connection density, and reduces interconnect delays.

3D industry research with TSV, thinned silicon, and silicon-silicon interconnections

As mentioned, demonstrations of emerging technologies making use of TSVs, thinned silicon, and high-density interconnection have been presented over the last 10 years. The 3D technology offers many potential advantages compared to traditional SoC or SiP technologies. For example, the distance between circuits for a 2D-only chip can be significantly reduced by using technologies involving two stacked dies. Use of TSV and fine-pitch interconnections can span six to eight orders of magnitude of chip interconnection density depending on structure [see Figure 1(b)] compared to traditional off-chip interconnection density having a span of about three orders of magnitude. Wafer processing can be simplified within one layer or strata of stacked silicon for a specific function such as processor or memory function instead of adding process steps for heterogeneous function in a 2D structure. The wide range of TSV and SSI densities and integration form factors can offer tradeoff options that may be matched for various product requirements even with heterogeneous chip integration.

This new 3D silicon technology is emerging at a time when Moore's Law for semiconductor chip scaling seems to be slowing or reaching an end [6, 26]. Technical

publications have described research including approaches for 3D ICs and chip stacking in which vertical vias and interconnections permit silicon-on-silicon stacking and high-bandwidth interconnection. From the late 1990s and early 2000s, many researchers studying 3D silicon integration have had technical publications reporting results and research progress from organizations such as the Association of Super-Advanced Electronics Technologies (ASET) Consortia of Japan and the Fraunhofer Institute of Germany. Research investigations have explored a wide variety of structures, processes, and bonding approaches. Researchers recognize the importance of 1) developing fine-pitch vertical interconnections using TSVs, 2) developing thinning technology for silicon and interconnection technology that joins thinned silicon dies into die stacks and that joins dies to silicon packages, and 3) developing wafer-to-wafer bonding technologies. In addition to power delivery and signal interconnections, investigators have also included approaches for thermal cooling and modeling of heat removal from thinned silicon structures and fine-pitch interconnections. Each 3D application will, of course, have its own integration challenges; however, common elements in the technology will generally require an understanding of power requirements for power delivery and cooling, interconnection density requirements, data-rate and bandwidth needs, and assembly methodology that can be influenced by chip and wafer interconnection, die and wafer yield, and test and reliability requirements.

Continuing improvements of interconnect technology is a key focus area and an enabler for the evolution of 3D IC design and packaging. As already indicated, TSV technology is one of the key interconnect solutions enabling a vertical method of electrical connectivity for various 3D IC configurations such as stacked die and wafer-level packaging. In TSV investigations, technical reports have included studies in which researchers sought submicron TSV diameters for compatibility with wafer front-end-of-line (FEOL) and back-end-of-line (BEOL) wafer fabrication or alternatively for silicon-based package solutions. TSV diameters and pitches have ranged from large sizes, such as about 10–100 μm via diameter and silicon thickness of about 50–300 μm , down to via diameters of less than 1–10 μm with corresponding silicon thicknesses ranging from about 50 μm down to about 1 μm silicon thicknesses, corresponding to those used in silicon-on-insulator (SOI) technologies. Reported TSV conductors have included tungsten, copper, composite, paste, doped polysilicon, as well as other electrical conductors. For example, Takahaski et al. [27] gave a TSV technical presentation on 10- μm copper conductors utilizing TSVs for electrical interconnection at a 20- μm pitch.

Fine-pitch interconnection, also at a 20- μm pitch for silicon-on-silicon connections with TSVs, has also been reported by Umemoto et al. [28]. Feil et al. [29] and Hutter et al. [30] have reported fine-pitch interconnection with a variety of bonding and electrical interconnection approaches between silicon die in thinned silicon die, die stacks, or packages using silicon. In these interconnection examples, anisotropic conductive polymers were used to bond 25- μm thinned dies with 50- μm -pitch AuSn bumps. Technical publications have also reported fine-pitch solder connections to copper as a means either to stack thinned silicon chips to other silicon dies or to join dies to silicon packages [28–31]. An application that leverages TSVs and fine-pitch interconnections with demonstration of functioning memory die stacks has also been presented by Ikeda et al. [32].

The main future challenge for TSV technology relates to its ability to maintain performance parameters, such as signal integrity or heat management, as data rates climb. However, a number of companies have been able to demonstrate efficient TSV electrical interconnect solutions that meet data rates on the order of 10 Gb/s. For example, Banpil Photonics indicated that its solution not only achieves high data rates (10 Gb/s and potentially up to 40 Gb/s) but also reduces power consumption up to 90% when compared to traditional solutions. Commercial availability of TSV technology is not expected prior to 2009 [33].

Other key enabling technologies for the continuing evolution of 3D IC design and packaging include solutions and equipment that support uniform Si thinning and precision alignment for wafer-to-wafer or chip-to-wafer bonding approaches. In this respect, the Sematech Advanced Technology Division continues to provide a forum through its 3D IC and packaging webcasts and workshops that highlight the state-of-the-art research and technical challenges related to deployment of new 3D interconnect solutions and costs associated with developing new materials, processes, and equipment for 3D integration. It engages key tool developers such as Semitool, Alcatell, or the EV Group in discussions of deliverable wafer processing 3D technology including TSV and SSI patterning, wafer thinning, and 3D alignment [34].

Uniform thinning of wafers, below 50 μm and down to the active layer, is a critical challenge. There are four primary methods for wafer thinning: 1) mechanical grinding, 2) chemical-mechanical polishing (CMP), 3) wet etching and atmospheric downstream plasma (ADP), and 4) dry chemical etching (DCE). Mechanical grinding provides the fast removal rate for Si but results in a damage region about 20 μm deep and a rough surface typically with a root-mean-square (rms) roughness of 2 μm . Therefore, the coarse grinding (with thinning rates

of $\sim 5 \mu\text{m/s}$) is usually followed by a fine grinding step (thinning rate $\leq 1 \mu\text{m/s}$), which removes most of the damage created by the coarse grinding step and reduces the roughness to a few nanometers depending on the wheel combination applied. To further polish the surface and remove a defect band (usually 0.1 μm in width or diameter and $\sim 1 \mu\text{m}$ deep) that remains after fine grinding near the surface, an additional thinning process can be implemented by CMP, dry etching, or wet chemical etching. CMP processing results in very flat surfaces and low total thickness variation (TTV) values; however, the thinning rate reaches values of only a few micrometers per minute and is optimized for sufficiently thick wafers ($\sim 200 \mu\text{m}$ or more, depending on the wafer size). Dry etching, especially using the Ar/CF₄ plasma process of Tru-Si Technologies, Inc., provides a thinning rate of about 20 $\mu\text{m}/\text{min}$, resulting in a variation of less than 2% after removing 20 μm of material. However, since this process exposes the surface to plasma, an amorphous layer about 0.2 μm thick and electrically active defects are created. On the other hand, wet chemical etching is one of the most common thinning techniques, and a typical etching rate for spin etching of silicon is about 10 $\mu\text{m}/\text{min}$. The TTV value depends on the etching time, the flow of the etching agent across the wafer surface, wafer rotation speed, and motion of the agent stream over the surface. The roughness of spin-etched silicon surfaces is less than 1 nm (rms) and, therefore, almost comparable to CMP processes. However, for the wet etching process, the minority-charge carrier lifetime (MCL)—a key parameter for FOEL applicability of the process—reaches high values compared to CMP processes. These values are also significantly higher than those of dry-etched materials.

Research related to controlled silicon thinning methods continues. This research focuses on manufacturability of this process and includes rapid controlled removal, surface restoration, and provision of temporary mounting techniques to enable further thin-wafer processing. The last solution is particularly critical, as many manufacturing tools, such as existing wafer-handling tools for 200-mm and 300-mm wafers, cannot handle thinned wafers below about 300 μm to 150 μm . Even limitations for thinned dies exist where 50 μm is often considered a limit below which the die may break during wire-bonding assembly operations. In most cases, 50 μm is regarded as the limit beyond which the wafer tends to often break down during tool operations. Also, at these small thicknesses, the electrical “punch-through” effects from one wafer to another can affect chip performance. Industry technologists believe that wafer thinning is a primary technical challenge for SiP growth, but it critically affects other packaging solutions. Hence, unless resolved, its impact on the ability to demonstrate 3D

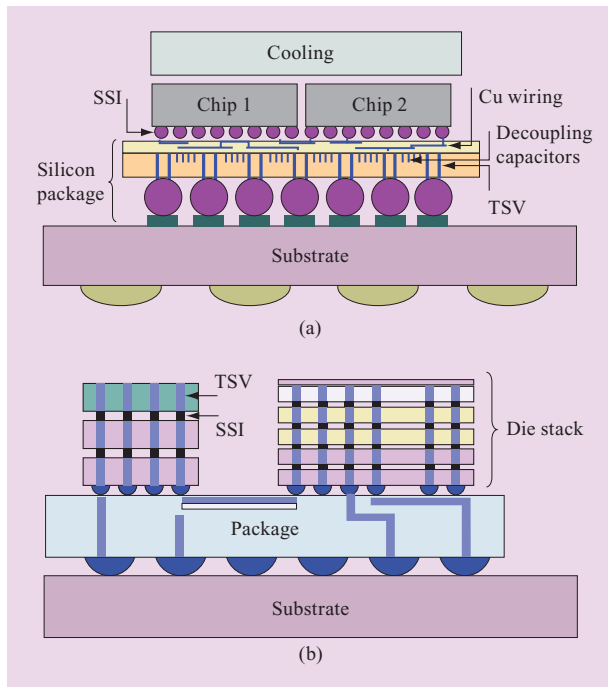


Figure 2

Schematic cross-sections for (a) a 3D Si package and (b) 3D die stacking. Oval structures at the bottom of part (a) represent a ball grid array, and the hemispheres at the bottom of part (b) represent C4 solder balls. The light green rectangle at the top of part (b) represents a microprocessor die, and the pink rectangle beneath it represents cache or a memory die. (SSI: silicon-silicon interconnection; TSV: through-silicon via.) (Republished from [35]; ©2008 IEEE.)

technology is expected to be high over the next few years [36].

3D research at IBM

At IBM, research on 3D integration with TSVs, thinned silicon, and fine-pitch silicon-silicon integration has been evolving for more than 10 years, and in the introduction, we briefly mentioned 3D test-vehicle designs and relevant studies. We note that for system integration, technology considerations include 1) design, 2) architecture, 3) design and modeling tools, 4) semiconductor technology, 5) package technology, 6) assembly technology, 7) test technology, 8) power delivery and cooling technology, 9) module form factor, and 10) reliability requirements. As mentioned, for 3D systems, we must consider design redundancy for interconnections, die size, manufacturing yield, cost, and test methodologies for manufacturing and product applications. In the next section, we report examples of test-vehicle designs, fabrication, and characterization at IBM Research with emphasis on die-stacking and silicon packaging 3D solutions.

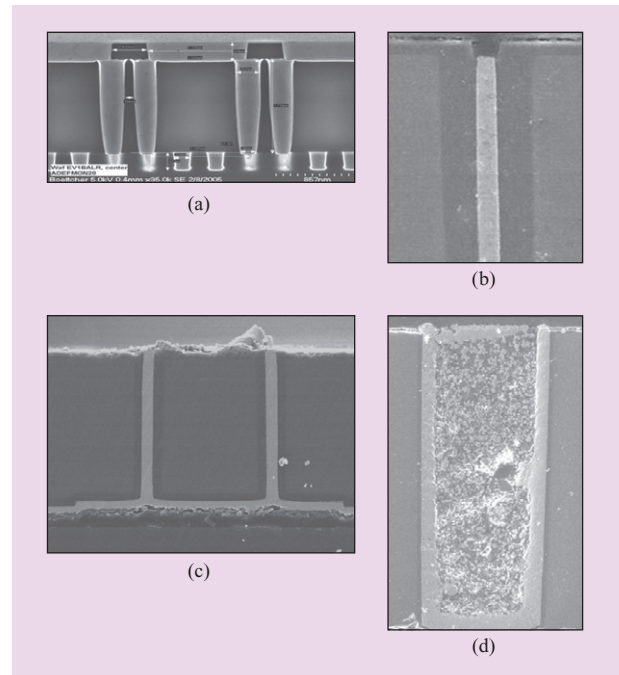


Figure 3

Examples of TSV cross-sections: (a) 0.14- μm -diameter TSV; (b) 2- μm -diameter TSV; (c) 70- μm annular via; (d) 70- μm composite via.

3D design and technology demonstration test vehicles

Advancement of 3D technology requires an understanding of the boundaries that affect its use. Thus, at its start, 3D design rules, physical structures, materials, processes, and tools must be explored to understand what may be possible as well as practical to meet targeted product, electrical, mechanical, and thermal objectives for products. Where TSV and SSI interconnection density targets are necessary, experiments need to be conducted to define practical ground rules for 3D technology.

Figure 2 shows two representative schematics for 3D silicon integration, including a silicon carrier for high-bandwidth integration between dies [part (a)], and die stacking with TSV and SSI interconnections [part (b)]. The wide range of technology elements (numbered 1 through 10 at the end of the previous section) must be considered when developing a 3D technology that goes far beyond existing design rules in use today. At the same time, developing practical design rules for applications needs to take into account materials, structures, processes, and tooling that can lead to a desired low-cost product with high yield. An approach was established to create data from test vehicles as a means to build a design

Table 1 Assembly and density comparison of silicon interconnection technologies. The term “rework” refers to the process in which a bad part can be replaced. (Adh: adhesive; S/C fab: semiconductor fabrication; redund: redundancy; KGD: known good die.)

Assembly technology	Bond	Approximate TSV and SSI pitch (μm)	Approximate I/O per cm^2	Approximate Si thickness (μm)	Compatible	Yield/options
Wafer to wafer						
SOI/face to back	Oxide or adhesive	20.0–0.4	10^5 – 10^8	4–2	S/C fab	Design/redundant
Bulk/face to face	Cu	20.0–5.0	10^5 – 10^6	20–5	S/C fab	Design/redundant
Bulk/face to back	Cu	20.0–10.0	10^5 – 10^6	20–5	S/C fab	Design/redundant
Chip to wafer						
Bulk/face to face	Cu or solder	200–5	10^5 – 10^6	70–10	Assembly	KGD/rework
Bulk/face to back	Cu or solder	200–10	10^5 – 10^6	70–10	Assembly	KGD/rework
Chip to chip						
Bulk/face to face	Cu or solder	200–5	10^5 – 10^6	70–10	Assembly	KGD/rework
Bulk/face to back	Cu or solder	200–10	10^5 – 10^6	70–10	Assembly	KGD/rework
Chip to Si package						
Bulk/face to face	Cu or solder	200–5	10^5 – 10^6	70–10	Assembly	KGD/rework
Bulk/face to back	Cu or solder	200–10	10^5 – 10^6	70–10	Assembly	KGD/rework

library, based on characterizations including reliability, that would complement successful structures and processes. Test demonstration vehicles used to develop 3D technology have included design, architecture, wafer fabrication, die-to-die assembly, die-to-wafer assembly, wafer-to-wafer assembly, fine-pitch tests, and characterizations including electrical, mechanical, thermal, and reliability assessments.

Test vehicles were developed for a wide range of studies important for 3D silicon integration. A few examples of test vehicles included 1) TSV test vehicles, 2) signal integrity characterization test vehicles, 3) CMOS-compatible TSV processes with integrated passive components test vehicles, and 4) SSI for assembly and reliability test vehicles.

TSV technology

TSVs are a critical enabler for both wafer-to-wafer and die-to-die stacking for which low-inductance, high-bandwidth vertical interconnects are needed in silicon. Applications may require only a few, thousands, or millions of vertical interconnections, a number that is very product dependent and is affected by architecture, desired product specifications, silicon thickness, materials, structures, and processes. Examples of TSV structures fabricated and characterized at IBM include TSVs that have a wide range of sizes, heights, aspect ratios, materials, densities and processes. For example, the range in size includes diameters or x/y sizes from less than $1 \mu\text{m}$ to $90 \mu\text{m}$. The silicon thickness ranges from

SOI thicknesses of less than $1 \mu\text{m}$ to a full wafer thickness of $730 \mu\text{m}$, with most studies having been performed with $150\text{-}\mu\text{m}$ thicknesses or less. Aspect ratios included evaluations from about 2-to-1 to more than 50-to-1 for thickness-to-diameter ratio or thickness-to-width ratio. Material evaluations have included copper, tungsten, and composite materials. **Table 1** provides examples of feature sizes and interconnection densities possible for several process options [21, 26, 37–40]. **Figure 3** shows examples of TSV cross-sections with different conductor materials, structures, and diameters from $0.14 \mu\text{m}$ to $70 \mu\text{m}$. Test-vehicle density evaluations have ranged from fewer than 10 TSVs per die to explorations of more than 10^6 TSVs per die. TSV processes studied have included versions of via-first, via-middle, and via-last processing (**Figure 4**). Via-first and via-middle TSV processing can be utilized by semiconductor and foundry fabricators. Via-middle and via-last processes may be utilized through collaboration between foundry and assembly companies, with each owning a portion of the process, for example, a foundry defining a landing pad and an assembly company creating the TSV conductor to make contact with the pad after wafer thinning from the backside of the wafer. Examples of process flow for TSV fabrication are shown in **Figure 4** where vias are etched with deep reactive-ion etching, insulated with thermal oxide, and then filled with liner and conductor. The via is opened after wafer thinning, and the bottom of the wafer is insulated and via contacted with backside metallization.

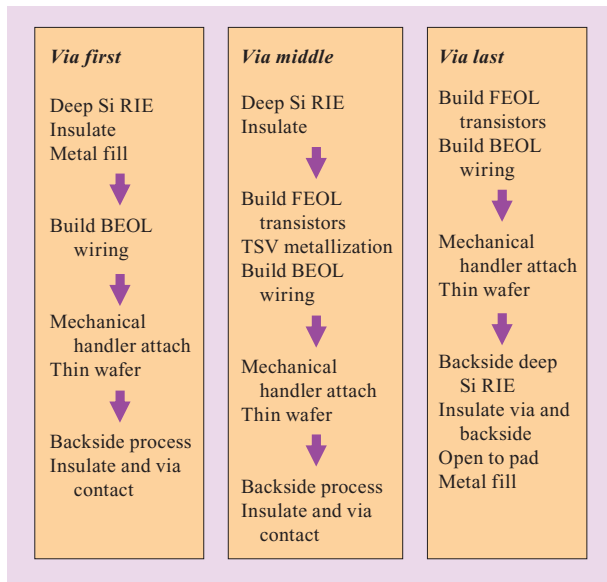


Figure 4

An example for process flow comparison for via-first, via-middle, and via-last processes. (RIE: reactive-ion etching; BEOL: back end of the line; FEOL: front end of the line; TSV: through-silicon via.)

3D electrical characterization test structures for TSV structures

For microelectronics and systems applications, signal integrity and power distribution requirements need to be considered when designing the 3D layouts for proper function at each silicon layer in the die stack and package. Schematic examples of demonstration test vehicles that permit different aspects of electrical characterization are shown in **Figure 5**. The two examples shown include [Figure 5(a)] a test structure for signal integrity, fine-pitch interconnection, and reliability stress characterization and [Figure 5(b)] a test structure for TSV and SSI interconnection or chip-stacking characterization; a test vehicle with TSV and integrated function is shown in Figure 2(a). Measurements, modeling, and simulation from these and other test vehicles have been crucial, and we reiterate that for 3D structures, signal integrity and power distribution are important considerations. Examples of time domain and frequency domain evaluations have been reported in the literature [21, 41, 42].

Coplanar waveguides were fabricated, characterized, and modeled. Characterization included feature sizes ranging from less than one to several microns for line widths and spaces. Results for each test structure are dependent on ground rules, structures, conductor materials, and process and assembly. In one test vehicle, measured results for TSVs showed an inductance at

0.15 pH/ μm thickness and resistance of 0.2 m Ω / μm thickness. Additional 3D signal integrity characterization and modeling has been undertaken through other test-vehicle designs, fabrications, and measurements. In these cases, design and characterization studies were conducted to evaluate signal integrity for finer-pitch TSVs and SSIs, for stacked silicon, for low-power interconnection, and to continue to expand a data library from a few microns to tens of microns for TSVs, SSIs, and for lines and spaces. Another test vehicle included coplanar waveguides of up to 75-mm line lengths and the ability to characterize low-power signal transmissions. Another test vehicle permits characterization of vertical signal integrity through TSVs and SSIs for fine-pitch vertical stacking. Results continue to be added to a reference database. Example results have included demonstration of high-speed transmission from 1 Gb/s to 10 Gb/s. For vertical stacking, the bandwidth between dies is dependent on the number of vertical interconnections and their frequency. For adjacent die-to-die interconnections, bandwidth is dependent on the number of connections, the length of connections, and frequency. Measured and simulated chip interconnections demonstrated that 8 Tb/s can be achieved for each wiring layer per centimeter of chip edge. More detailed examples of signal integrity characterization are reported by Patel [42].

Power delivery and cooling also need to be taken into account in 3D structure design. A variety of options may be considered for uniform power distribution across many silicon levels in a 3D structure operating at low voltage. For example, depending on the number of voltages to be supported, voltage levels, and number of layers, options may include localized voltage regulators, voltage transformation or inversion, power decoupling capacitors, power plane segmentation, and size hierarchy of power grids [35, 43]. Test vehicles to further study close-proximity, low-inductance, integrated decoupling capacitors were designed, fabricated, and assembled with trench decoupling capacitors and TSVs, as is schematically shown in Figure 2(a) and physically shown in **Figure 6(a)** as an expanded and open module and in **Figure 6(b)** as a cross-section. The test vehicles employed segmented voltage planes to support multiple voltage levels that were tied to corresponding banks of decoupling capacitors. Some test vehicles were targeted for module-level assembly and characterized for performance with and without the 3D-stacked silicon decoupling capacitor. Other test vehicles were used to characterize silicon- and module-level reliability. Results showed that a single level of deep trench decoupling capacitors provided a capacitance of 12–14 microfarads/cm² [35]. Additional test-vehicle designs, fabrication, and characterization are planned.

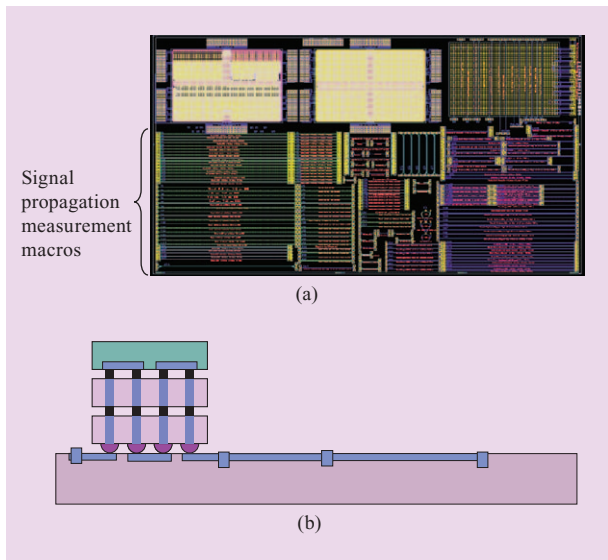


Figure 5

Examples of (a) a signal integrity test vehicle (i.e., a schematic or layout for the chip) for frequency and time domain characterization and (b) a chip-stack characterization test vehicle. A multichip test vehicle with integrated decoupling capacitors is shown in Figure 2(a).

SSI technology and module integration

SSI investigations for 3D circuit integration have ranged from studies of SOI structures [20], to thin die stacks using face-to-face or face-to-back structures [38, 39], to silicon stacking [44], and silicon-on-silicon packages [21, 45, 46]. Across these interconnection studies, assessments have included oxide-to-oxide bonding, copper-to-copper interconnection, and solder interconnection for vertical SSI. Table 1 compares the relative attributes and merits of these technologies.

Another aspect of SSI that must be considered is the ability to process the structures, test, and assemble them. The approach to best optimize yield and manufacturing can be dependent on the application, design, die size, die and wafer yield, interconnection density, alignment specifications, bonding or assembly yield, and ability to test at various stages of fabrication. **Figure 7** compares pros, cons, and other aspects of chip-to-chip assembly, chip-to-wafer bonding, and wafer-to-wafer bonding for solder, copper, and oxide bonding.

Advantages of chip-to-chip processing include the ability to have known good dies for improved die-stack yields. Advantages of die-on-wafer (i.e., chip-to-wafer) processing can include lower costs for wafer-level processing, also using known good dies for assembly. Wafer-to-wafer processing can provide the ultimate solution for manufacturing if die and wafer yields are

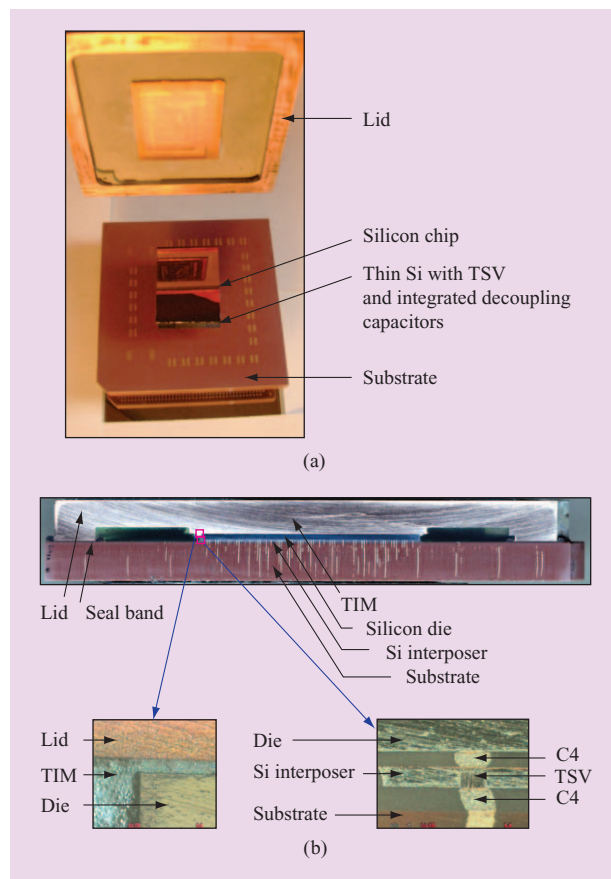

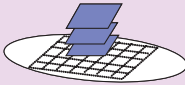
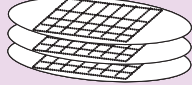


Figure 6

Demonstration test vehicle with TSVs and integrated decoupling capacitors: (a) an expanded and open view of a package, thinned silicon decoupling capacitor, die, and cap prior to assembly; (b) a cross-section of an assembled die stack with integrated Si decoupling capacitor. (TIM: thermal interface material; C4: controlled-collapse chip connection.)

extremely high or a redundancy scheme is utilized to avoid loss of stacked die. The disadvantages of chip-to-chip and chip-to-wafer processing include difficulties and costs associated with handling and bonding individual dies, whereas the difficulty with wafer-to-wafer processing involves an overall lower yield.

Advantages of solder interconnection include high yields for assembly and extension of known technology, industry infrastructure, testing, and rework. Here, the size and interconnection density that can be supported continue to scale to smaller dimensions in industry use as well as with demonstrations at IBM that include diameters of 5–10 μm [30, 47, 48]. Disadvantages of solder are the added cost for underbump metallurgy (UBM) or solder and the incompatibility with solder in a wafer process line.

	<i>Chip to chip</i> 	<i>Chip to wafer</i> 	<i>Wafer to wafer</i> 
<i>Pros</i>	Flexible, use of KGD	Flexible, use of KGD	Low cost
<i>Cons</i>	Handling and bonding	Handling and bonding	Overall yield, chip size
<i>Wafer thickness</i>	<4 μm to >150 μm	<4 μm to >150 μm	<4 μm to >150 μm
<i>Bonding technology</i>	Solder Metal to metal Adhesive	Solder Metal to metal Adhesive	Solder or metal-oxide bonding Adhesive


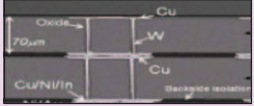
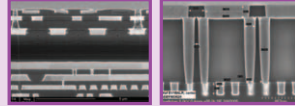
 <p>Chip-to-chip bonding C4 solder or microbumps</p>	 <p>Chip-to-wafer bonding Thin solder/intermetallic</p>	 <p>Wafer-to-wafer bonding Cu-to-Cu or oxide bonding</p>
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Figure 7

Silicon–silicon interconnection comparison for chip-to-chip assembly, chip-to-wafer bonding, and wafer-to-wafer bonding with solder, thin-metal, copper–copper, and oxide-to-oxide bonding. (KGD: known good die.) (Adapted with permission from [35]; ©2008 IEEE.)

3D electrical characterization test structures for SSI structures

Fine-pitch SSI test vehicles have been designed, fabricated, and characterized (Table 1). For wafer-scale integration of circuits including wafer thinning, alignment and bonding results for the interconnections between silicon levels yielded dimensions of as small as approximately 0.14 μm for diameter, 1.6 μm for height, and 0.4 μm for pitch. Interconnection densities of $10^8/\text{cm}^2$ were previously reported [38, 40, 49] [Figure 3(a) and Figure 7]. Some wafer test structures have had an interconnection pitch of 20 μm . When examined for wafer-scale interconnection, the range in numbers of interconnections for alignment and bonding or integration for pitches from 0.4 μm to 20 μm could be from 70 billion to 175 million connects between thinned silicon wafer levels.

IBM test-vehicle demonstrations have been used to evaluate chip-to-chip stacking, chip-to-wafer stacking, and silicon packages. Experiments were conducted with copper-to-copper interconnection, solder interconnection or microbumps, and thin-solder and/or intermetallic interconnections [21, 42, 45, 46, 48, 49] (Figure 7). In these test vehicles, interconnection sizes included dimensions of approximately 4- μm diameter on 10- μm pitch, 10- μm diameter on 20- μm pitch, 20–25 μm on 50- μm pitch, 50 μm on 100- μm pitch, and 100 μm on

200- μm pitch. Interconnection height ranged from 2 to 75 μm and density from $10^3/\text{cm}^2$ to $10^6/\text{cm}^2$. In these test demonstrations, TSVs in test structures included diameter or width sizes of approximately 2 μm , 3–8 μm , 25 μm , 50 μm , 70 μm , and 90 μm . Pitches included 12 μm , 50 μm , and 200 μm . The TSV and/or I/O interconnections included approximately 2,160, 5,000, 10,000, 52,000, and 350,000 per die or test structure with or without built-in redundancy. **Figure 8** shows an example of 25- μm -diameter solder microbumps at different magnifications. For example, one solder bump is shown in Figure 8(a), and Figure 8(b) shows a 300-mm wafer with an area array of solder microbumps formed by C4NP (controlled-collapse chip connection new process), which is a low-cost solder injection process that first fills a mold with solder and then transfers this to the wafer. C4NP permits high-volume manufacturing wafer processing at a low cost with precise control of solder composition. See Figures 8(c) and 8(d) for other microbump arrays. At 50- μm pitch, a fully populated 300-mm wafer could have more than 28 million solder microbumps, and scaled to 10- μm pitch, a 300-mm wafer could contain more than 700 million interconnections.

Figures 9(a) and **9(b)** show examples of a silicon-on-silicon, two-high stack mounted on an organic package using solder interconnections. **Figures 9(c)** and **9(d)** show small-height interconnection joining for six-high thinned

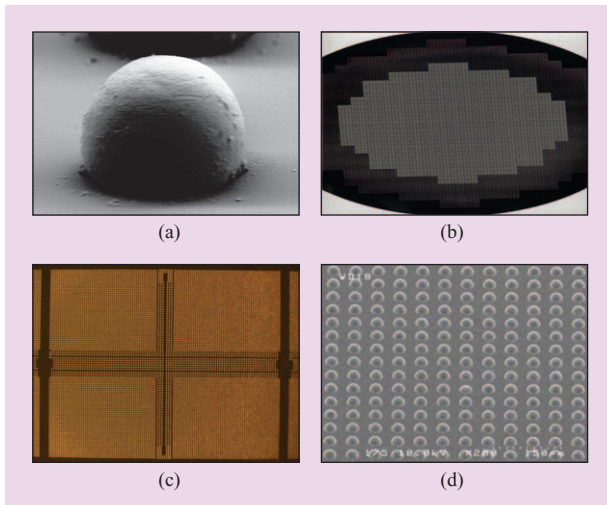


Figure 8

Fine-pitch interconnections including (a) a single $\sim 25\text{-}\mu\text{m}$ -diameter microbump, (b) a 300-mm wafer with microbumps at $50\text{-}\mu\text{m}$ pitch formed by C4NP (controlled-collapse chip connection new process), having potential for ~ 28 million microbumps, (c) an array of $\sim 40,000$ microbumps/cm², and (d) an array of ~ 192 microbumps.

silicon-to-silicon die stacks on a silicon wafer [48–50]. Results showed that 100% good assemblies could be fabricated, and the structures were characterized for electrical parametrics, mechanical parametrics, and physical and reliability characteristics.

Known good dies and reliability testing

Known good dies can be obtained from pretesting die at the wafer level or from statistical testing. Alternatively, die stacks can be created using redundant interconnections to aid in wafer-stacking or die-stack yields. To demonstrate a test methodology for known good dies with fine-pitch interconnections, test probes were fabricated at a $50\text{-}\mu\text{m}$ pitch, and corresponding microbumps were successfully contacted as previously reported [21].

Reliability testing for fine-pitch interconnections has also continued to be studied through the use of demonstration test vehicles. For example, electrical continuity tests of microbump chains showed that the 20- to $25\text{-}\mu\text{m}$ -diameter microbumps had approximately 5–26 m Ω resistance, depending on the test structure used [46]. Reliability studies for $50\text{-}\mu\text{m}$ -pitch solder microbumps produced electromigration results for more than 2,000 hours for 100-mA current at 125°C and 150°C, deep thermal cycle results of more than 25,000 cycles from -55°C to $+125^\circ\text{C}$, temperature-humidity bias of

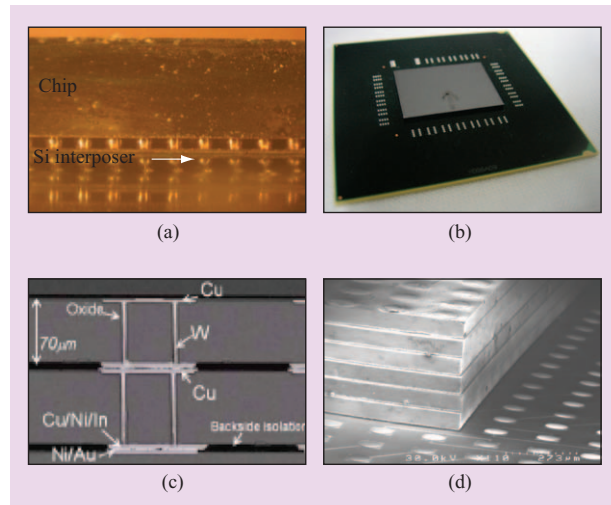


Figure 9

Examples of silicon-silicon stacking or “die stacking”: (a) A single chip is mounted on thinned $70\text{-}\mu\text{m}$ -thick interposer using solder interconnections; (b) a chip and thinned silicon stack are on an organic package; (c) cross-section with through-silicon via and thinned interconnection; (d) thinned, stacked silicon test structures on a wafer.

more than 1,000 hours for 85°C, 85% relative humidity, and 1.5 V, and more than 2,000 hours of high-temperature storage at 150°C [21, 46]. Results indicate that fine-pitch interconnections can be fabricated and meet typical product reliability stress requirements. Data in **Figure 10** shows results from microbump electrical and mechanical shear testing as a function of pad size [48]. Further studies of multichip and die-stack test structures with increased interconnection densities between $10^3/\text{cm}^2$ and $10^8/\text{cm}^2$ for TSVs and SSIs are at various stages of design, build, and characterization and will permit ongoing experiments and data to be investigated, including design rules, process, bonding, and test structure characterization and methodology. These ongoing investigations in wafer-to-wafer processing as well as chip-to-wafer and chip-to-chip interconnection will continue to provide data that will permit interconnection density, materials, structures, and processes to be optimized for manufacturing considerations and applications. Data collected can provide guidance to help meet application reliability objectives for TSVs, SSIs, and a variety of integrated module form factors that permit system miniaturization.

3D systems and applications

New products that incorporate these emerging 3D silicon integration technologies will be used for applications that

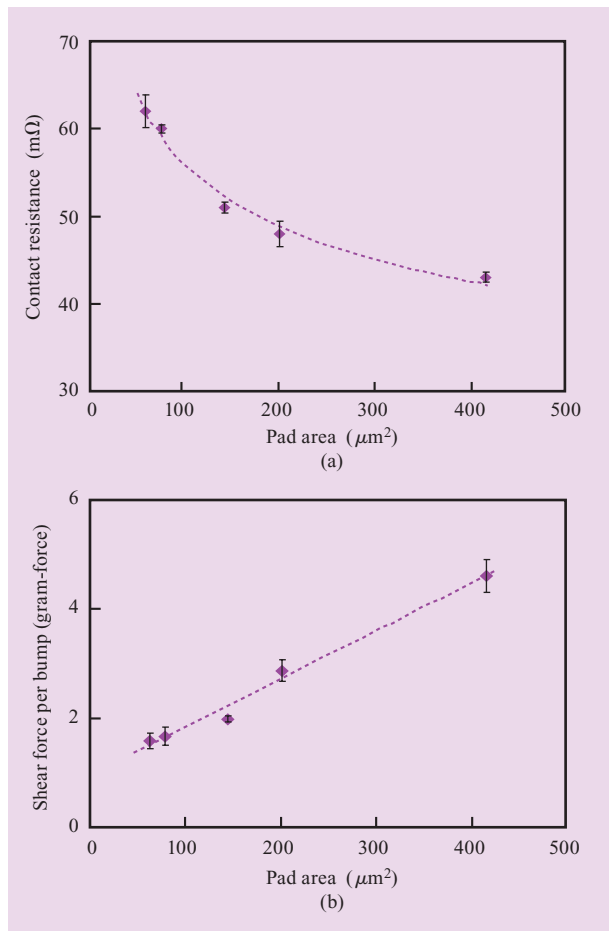


Figure 10

Electrical and mechanical interconnection results: (a) silicon-on-silicon electrical contact resistance when joined to various pad sizes; (b) silicon-on-silicon mechanical shear results when joined to various pad sizes.

create business value. Creation of business value or product value may take different forms such as 1) improved system performance, 2) increased power efficiency, 3) lower system cost, 4) improved time to market, or 5) improved product form factors such as through miniaturization. In addition, new products and integrated classes of products may become viable through heterogeneous integration, and such possibilities were not previously possible based on prior technology integration.

For computing applications, 2D system-scaling challenges are increasing with lithographic advancements and with the slowing of Moore's Law [26]. Parallel computing can help support system performance scaling with the use of multicore dies and multithread software solutions. For lithographic features, reductions challenges

include increasing power requirements due to gate leakage and increased use of repeaters as wire sizes decrease. For multicore dies, power savings can be realized through operation at a scaled-back frequency; however, as the number of multicore dies grows, the bandwidth to cache and memory must scale substantially [51]. System challenges and semiconductor scaling limits need not limit system scaling or improved power efficiencies. For example, to complement semiconductor advancements, subsystem scaling using 3D, high-performance die stacks and packages can facilitate system advancements. The subsystem scaling can include 3D integration with high-bandwidth electrical and optical interconnection between large numbers of multiprocessor cores and cache memory [22, 51, 52]. Appropriate architecture and software that can leverage these 3D multicore, multithreaded structures will also be critical to optimize the benefit for system scaling ahead of the potential future post-CMOS technology and quantum computing technology solutions [26, 52]. Another challenge for computing applications is cooling. Similar to prior power-density escalations over a decade ago in semiconductor technology solutions using bipolar transistors, current CMOS transistors are once again creating high power densities that need to be addressed [53]. Three-dimensional technology may provide a means to help reduce power consumption not only with scaled-back frequency operation for multicore processors but also through shorter-distance interconnections that require reduced power for signal communications between circuits.

For other product applications, 3D technology potential benefits such as cost, power efficiency, performance, and size are likely to lead to a variety of new product applications. A wide range of integration solutions is possible, such as simple wireless dies with fewer than 10 TSVs and applications such as image sensors with 3D die stacks requiring high-density interconnections between layers. First products are entering production in 2008, including power amplifier dies from IBM for wireless applications [54] and image sensors from Toshiba [55, 56]. Another example of 3D applications is memory chip stacks for which thinned DRAMs have been demonstrated [37, 51, 57]. Wider industry adoption and acceleration of product applications are likely with the adoption of 300-mm tools such as deep silicon reactive-ion etching, thin-wafer handling, and alignment and bond tools. To gain the greatest leverage for more complex products, product architects will need to understand how to leverage the full potential for 3D silicon integration for specific applications. Meanwhile, process engineers will need to develop processes and corresponding design rules that permit high-yield and 3D integration approaches that can

support the targeted range of product applications at competitive costs.

Given time to mature, applications for 3D integration will be far reaching. Examples may include portable electronics such as cell phones, portable medical products, and portable sensors. With the reduced power consumption, portable products may benefit from enhanced battery life, reduced size, and increased function. Additional applications may include military, information technology, communications, automotive, and space applications. For computing applications, memory chip stacks for high-bandwidth integration with microprocessors may provide reduced power, system performance scaling, and smaller products. In addition, it is likely that new applications and products will emerge given the advancements in these microelectronics technologies, nanoelectronics technologies, and emerging biotechnologies as well as other emerging nanotechnologies. It seems clear that the industry is just beginning to consider new applications and products that may take advantage of 3D silicon integration.

Summary

Emerging 3D silicon integration technologies using TSVs, thinned silicon, and SSIs have the potential to be used in a broad range of applications. Technology advancements and implementation using 200-mm and 300-mm tools are growing in the industry. IBM continues to drive technology advancements in research through design, fabrication, and characterization of test-vehicle demonstrations. In addition, IBM is supporting customer applications as the technology advances through technology qualifications. Future product applications will rely on new product applications, new architectures, and various approaches for creating business value.

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