LIST OF FIGURES

CHAPTER ONE: INTRODUCTION

1.1. Computer System Hardware Block Diagram
1.2. Operator Interaction with Computer System Flow Chart
1.3. Queueing Network Block Diagram
1.4. Scheduler Flow Chart
1.5. Illustrative Time Epochs for Processing a Job
1.6. Upper and Lower Bounds on Mean Throughput Rate
1.7. Upper and Lower Bounds on Mean Response Time
1.8. Layered Model of Computer System
1.9. Application Program Development Flowchart
1.10. Program Development Block Diagram
1.11. Round Robin Queueing Network Block Diagram
1.12. Local Area Network Hardware Interface Block Diagram
1.13. Work Station to Local Area Network Data Transfer
1.15. Hardware Block Diagram
1.16. States of a Process
1.17. Illustrative Set of Processes Managed by Operating System
1.18. Operating System Network of Queues
1.19. Processor Block Diagram
1.20. Processor Instruction Execution Flow Chart
1.21. Bit Transmission Probabilities
1.22. Three Stage (N=3) Processor Pipeline
1.23. Multiple Processor Multiple Memory Hardware Block Diagram
1.24. Hardware Block Diagram
1.25. Electronic Mail Pending Flow Chart

CHAPTER TWO: CONCURRENCY AND PARALLELISM

2.1. Pipeline and Parallel Configurations
2.2. Arithmetic Logic Unit Block Diagram
2.3. Floating Point Accelerator Block Diagram
2.4. SPT/NP Single Slow Printer Schedule
2.5. LPT/NP Single Slow Printer Schedule
2.6. SPT/NP Two Slow Printer Schedule
2.7. LPT/NP Two Slow Printer Schedule
2.8. SPT/NP Schedule for One Slow Printer (10,000 Lines for Job J)
2.9. LPT/NP Schedule for One Slow Printer (10,000 Lines for Job J)
2.10. SPT/NP Schedule for Two Slow Printers (10,000 Iines  
2.11. LPT/NP Schedule for Two Slow Printers (10,000 Iines  
2.12. Illustrative Operation: Number of Busy Set  
2.13. A. Three Processor Nonpreemptive Schedul 
2.13. B. A Preemptive Schedule for Three Proc: 
2.14. Schedule One for Three Processors  
2.15. Schedule Two for Three Processors  
2.16. Illustrative Comparison of Deadline vs Stat  
2.17. Three Stage Pipeline  
2.18. Three Stage Pipeline Schedule for Six Jobs  
2.19. Schedule One Processor Activity (P=3,N=3  
2.20. Schedule Two Processor Activity (P=3,N=3)  
2.21. Two Stage Pipeline  
2.22. Precedence Constraints for Six Jobs  

CHAPTER THREE: A ANALYSIS AND SIMULATION 93  
3.1. Statistical Measures  
3.2. Printer Activity Using Alphabe Priorities  
3.3. Shortest Processing Time Prior Arbitratic  
3.4. Empirical Distribution Function  
3.5. Histogram of Directory Assist  
3.6. Erlang 1 vs Data Q-Q Plot  
3.7. Erlang 2 vs Data Q-Q Plot  
3.8. Erlang 3 vs Data Q-Q Plot  
3.9. Erlang 4 vs Data Q-Q Plot  
3.10. Erlang 5 vs Data Q-Q Plot  
3.11. Representative Timing Diagram of a Simulation  
3.12. Communications Link Hardware Block Diagram  
3.13. Communications Link Queuing Network Block Diagn 
3.14. GPSS Link Flow Control Simulation  
3.15. Interarrival Time Empirical Cumulative Distribution uncti  
3.16. Offset and Dialtone Generation Steps  
3.17. Digit Dialing and Billing  
3.18.  
3.19. C  
3.20.  

CHAPTER FOUR: MEAN VALUE ANALYSIS 140
LIST OF FIGURES

4.2. Number of Jobs in System vs Time 143
4.3. Hardware Block Diagram of Time Sharing System 146
4.4. Mean Throughput Rate Bounds vs Number of Active Users 146
4.5. Mean Response Time Bounds vs Number of Active Users 149
4.6. Telephone System Block Diagram 151
4.7. Hardware Block Diagram of Serial and Concurrent Processors 154
4.8. Packet Network Block Diagram 156
4.9. Processor and Disk Hardware Block Diagram 156
4.10. Queueing Network Block Diagram 159
4.11. One Processor/One Disk Mean Throughput Bounds 159
4.12. One Processor/One Disk Mean Response Time Bounds 163
4.13. Block Diagram of Memory Constrained Queueing Network 168
4.15. Hardware Block Diagram of Record Processing System 177
4.16. Distributed Data Communications System Block Diagram 177
4.17. Queueing Network Block Diagram 186
4.18. Admissible Mean Throughput Rates 206

CHAPTER FIVE: OFFICE COMMUNICATIONS

5.1. Telephone Tag Work Flow 207
5.2. Voice Storage Work Flow 210
5.3. Office Copying System Block Diagram 212
5.4. Queueing Network of Office Copying System 212
5.5. Mean Document Copying Rate 214
5.6. Document Preparation System Hardware Block Diagram 215
5.7. Document Preparation Queueing Network Block Diagram 216
5.8. Existing Old System Hardware Block Diagram 220
5.9. Proposed New System Hardware Block Diagram 221
5.10. Old System Professional Work Flow 224
5.11. New System Professional Work Flow 228
5.12. Office Block Diagram 229
5.15. Telephone Message Handling Block Diagram 239
5.16. Feasible Set of Mean Throughput Rate 240
5.17. Mean Document Completion Rate vs Number of Secretaries 241
5.18. Mean Document Waiting Time vs Number of Secretaries
CHAPTER SIX: JACKSON NETWORK ANALYSIS

6.1. System Block Diagram
6.2. Queueing Network Block Diagram
6.3. Partition Function FORTRAN Program
6.4. Mean Throughput Rate vs Number of Clerks
6.5. Mean Delay vs Number of Clerks
6.6. Erlang Blocking Function FORTRAN Program
6.7. Call Distributor Block Diagram
6.8. Call Distributor Queueing Network Block Diagram
6.9. System Block Diagram
6.10. Queueing Network Block Diagram
6.11. Mean Throughput Rate vs Degree of Multiprogramming
6.12. Pipeline Queueing Network Block Diagram
6.13. Mean Throughput Rate vs Mean Processor Time/Query
6.14. Mean Response Time vs Mean Processor Time/Query

CHAPTER SEVEN: ACKSON NETWORKS: APPLICATIONS

7.1. Hardware Block Diagram of Communications Link
7.2. Queueing Network Block Diagram of Communications Link
7.3. Mean Throughput Rate vs Buffers \( T_{prop} = 0.1 \)
7.4. Mean Throughput Rate vs Buffers \( T_{prop} = 1.0 \)
7.5. Mean Throughput Rate vs Buffers \( T_{prop} = 10.0 \)
7.6. Maximum Mean Throughput Rate vs Buffers \( T_{trans} = 1.0 \)
7.7. Maximum Mean Throughput Rate vs Buffers \( T_{trans} = 0.5 \)
7.8. Maximum Mean Throughput Rate vs Buffers \( T_{trans} = 0.2 \)
7.9. A. Transmitter Simulation Results
7.9. B. Receiver Simulation Results
7.10. Mean Throughput Rate Bounds vs Buffers \( T_{rec} = 1.0, T_{trans} = 1.0 \)
7.11. Mean Throughput Rate Bounds vs Buffers \( T_{rec} = 1.0, T_{trans} = 0.5 \)
7.12. Mean Throughput Rate Bounds vs Buffers \( T_{rec} = 1.0, T_{trans} = 0.2 \)
7.13. An Illustrative Communications Network
7.14. L Uncoupled Links
7.15. General Network with N Ports and L Links
7.16. An Illustrative Tree Network
7.17. Circuit Switching System Hardware Block Diagram
7.18. Circuit Switching System Queueing Network
7.19. Blocking vs Mean Arrival Rate (R = 1)
7.20. Blocking vs Mean Arrival Rate (R = 2)
7.21. Mean Throughput Rate vs Mean Arrival Rate (R = 1)
LIST OF FIGURES

7.22. Mean Throughput Rate vs Mean Arrival Rate (R=2)  344
7.23. PROB[T_w > 3] vs Mean Arrival Rate (R=1)  345
7.24. PROB[T_w > 3] vs Mean Arrival Rate (R=2)  345
7.25. Blocking vs Mean Arrival Rate (R=1)  347
7.26. Blocking vs Mean Arrival Rate (R=2)  347
7.27. Mean Throughput Rate vs Mean Arrival Rate (R=1)  348
7.28. Mean Throughput Rate vs Mean Arrival Rate (R=2)  348
7.29. PROB[T_w > 1] vs Mean Arrival Rate (R=1)  349
7.30. PROB[T_w > 1] vs Mean Arrival Rate (R=2)  349
7.31. Digital Circuit Switching System  351
7.32. State Space of Variable Bandwidth 2.4/4.8 KBPS Switch  357
7.33. Two Input Links/One Switch/Two Output Links  358
7.34. Blocking vs Balanced/Unbalanced Load  359
7.35. Variable Bandwidth Circuit Switch  360
7.36. Blocking vs Low Bandwidth Offered Load  361

CHAPTER EIGHT: JACKSON NETWORKS: APPLICATION II  368

8.1. PBX Hardware Block Diagram  369
8.2. PBX Queueing Network Block Diagram  370
8.3. Packet Switching System Hardware Block Diagram  375
8.4. Packet Switching System Data Flow Block Diagram  375
8.5. Packet Switching System Queueing Network Block Diagram  377
8.6. Automatic Call Distributor with Customer Defection  387
8.7. Processor/Memory Hardware Block Diagram  391
8.8. Process Contention for Operating System Table  392
8.9. Processor/Disk Hardware Block Diagram  392
8.10. Clerk/System Block Diagram  393
8.11. Hardware Configuration  399
8.12. Queueing Network Block Diagram  400
8.13. Mean Throughput Rate vs Number of Lines/Clerk  401
8.14. Mean Customer Delay vs Number of Lines/Clerk  402
8.15. Trouble Entry Work Flow  403
8.16. Trouble Report Work Flow  404
8.17. Trouble Tracking Work Flow  405

CHAPTER NINE: PRIORITY SCHEDULING  423

9.1. Empirical Quantiles vs Exponential Model Quantiles  426
9.2. Empirical Quantiles vs Exponential Model Quantiles  432
LIST OF FIGURES

9.3. Hyperexponential Random Variable Generation 434
9.4. Hyperexponential Distribution Flow Chart 435
9.5. Illustrative Link Operation \((T_{prop} = 0)\) 436
9.6. Mean Throughput Gain of Double vs Single Buffering 438
9.7. Fraction of Time \(T_Q > X\) vs \(X\) 443
9.8. Mean Throughput Rate vs Mean Arrival Rate 445
9.9.A. Mean Waiting Time vs Utilization \((\rho \leq 1)\) 448
9.9.B. Mean Queueing Time vs Utilization \((\rho \leq 1)\) 449
9.9.C. Mean Number in System vs Utilization \((\rho \leq 1)\) 449
9.10.A. Mean Waiting Time vs Utilization \((\rho \leq 0.5)\) 449
9.10.B. Mean Queueing Time vs Utilization \((\rho \leq 0.5)\) 450
9.10.C. Mean Number in System vs Utilization \((\rho \leq 0.5)\) 450
9.11.A. Fraction of Time \(T_Q > X\) vs \(X\) 451
9.11.B. Fraction of Time \(T_W > X\) vs \(X\) 451
9.11.C. Fraction of Time \(N > K\) vs \(K\) 452
9.12. PROB \([T_Q > X]\) vs \(X\), LCFS/PR/Constant Service 456
9.13. PROB \([T_Q > X]\) vs \(X\), LCFS/PR/Exponential Service 457
9.14.A. PROB \([T_Q > X]\) vs \(X\), FIFO and LCFS/NP and LCFS/NP 458
9.14.B. PROB \([T_Q > X]\) vs \(X\), FIFO and LCFS/NP and LCFS/NP 459
9.15. SDLC Frame Format 462
9.16. SDLC Priority Arbitration Queueing Network Block Diagram 462
9.17. Illustrative Bit Stuffing Example: \(D=13, R=2\) 463
9.18. Illustrative Spurious Flag from Single Bit Error 463
9.19. SDLC Link Controller Block Diagram 464

CHAPTER TEN: PRIORITY SCHEDULING II 473

10.1. Packet Switching System Work Flow 474
10.2. Nonpreemptive Static Priority Scheduling 477
10.3. Controlled Nonpreemptive Scheduling 477
10.4. Multiple Level Downward Migration Scheduling 478
10.5. Interrupt Driven Preemptive Resume Scheduling 478
10.6. General Static Priority 479
10.7. Best Case Nonpreemptive Scheduler: \(\text{PROB}[T_Q > X] vs X\) 490
10.8. Worst Case Nonpreemptive Scheduler: \(\text{PROB}[T_Q > X] vs X\) 491
10.9. Mean Queueing Time vs Service Time Required 495
10.10. Illustrative Cost Functions vs Time 500
10.11. Admissible Region of Mean Waiting Time Vectors 501
10.12. Link Level Multiplexer 507
10.13. An Illustrative Frame 507
CHAPTER ELEVEN: LOCAL AREA NETWORKS

11.1. Topology of a Local Area Network
11.2. Mean Packet Delay vs Arrival Rate
11.3. Circuit Switching Local Area Network
11.4. Packet Switching Local Area Network
11.5. Broadcast Bus Local Area Network
11.6. Ring Local Area Network
11.7. Illustrative Token Bus Operation
11.8. Mean Throughput Feasible Region
11.9. Mean Delay vs Number of Stations
11.10. $E(T_{Q1})$ vs Total Bus Utilization
11.11. $E(T_{Q2})$ vs Total Bus Utilization
11.12. $E(T_{Q1})$ vs Total Bus Utilization
11.13. $E(T_{Q2})$ vs Total Bus Utilization
11.14. Mean Message Waiting Time vs Bus Utilization
11.15.A. Mean Queueing Time vs Link Utilization ($N=20$)
11.15.B. Mean Queueing Time vs Link Utilization ($N=100$)
11.16. Illustrative Operation of CSCD
11.17. Maximum Mean Throughput Rate vs Clock Rate
11.18. Mean Message Delay Upper Bound vs Utilization
11.19. Mean Message Delay Upper Bound vs Utilization
11.20. Reservation Decision Tree Access
11.21. Reservation Tree Access: Order of Arrival
11.22. Reservation Tree for Order of Arrival
11.23. Maximum Mean Data Rate vs Clock Rate
11.24. Maximum Mean Data Rate vs Clock Rate
11.25. Lower Bound on Message Delay vs $N$